24 Analog/digital converter (ADC)

24.1 Introduction

ADC1 and ADC2 are 10-bit successive approximation Analog to Digital Converters. They have up to 16 multiplexed input channels (the exact number of channels is indicated in the datasheet pin description). A/D Conversion of the various channels can be performed in single, and continuous modes.

ADC1 has extended features for scan mode, buffered continuous mode and analog watchdog. Refer to the datasheet for information about the availability of ADC1 and ADC2 in specific product types.

24.2 ADC main features

These features are available in ADC1 and ADC2.

- 10-bit resolution
- Single and continuous conversion modes
- Programmable prescaler: f_{MASTER} divided by 2 to 18
- External trigger option using external interrupt (ADC_ETR) or timer trigger (TRGO)
- Analog zooming (in devices with V_{REF} pins)
- Interrupt generation at End of Conversion
- Data alignment with in-built data coherency
- ADC input range: $V_{SSA} \leq V_{IN} \leq V_{DDA}$

24.3 ADC extended features

These features are available in ADC1.

- Buffered continuous conversion mode(1)
- Scan mode for single and continuous conversion
- Analog watchdog with upper and lower thresholds
- Interrupt generation at analog watchdog event

The block diagrams of ADC1 and ADC2 are shown in *Figure 154* and *Figure 155*

1. Data buffer size is product dependent (10 x 10 bits or 8 x 10 bits). Plese refer to the datasheet.

Figure 154. ADC1 block diagram

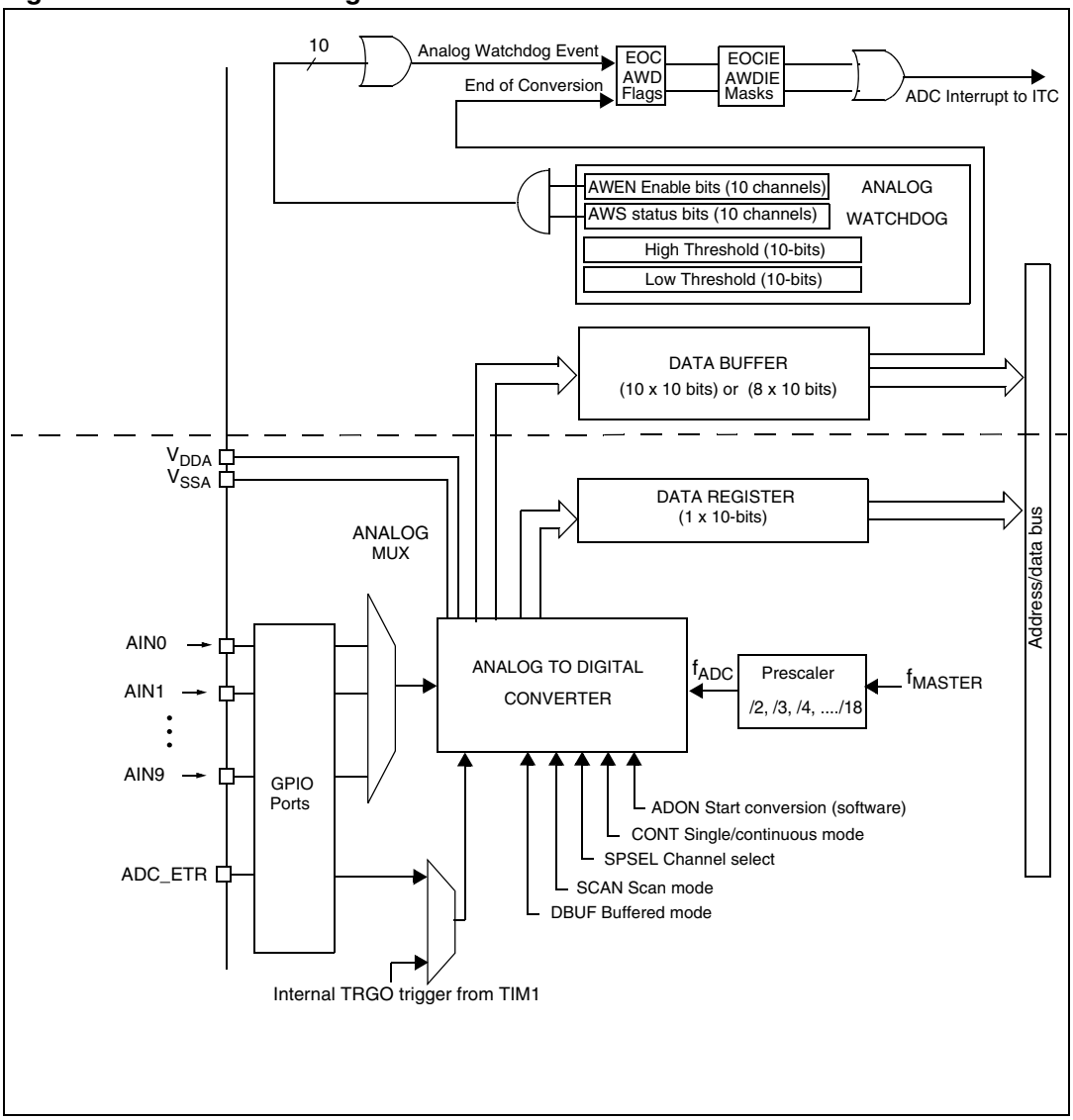
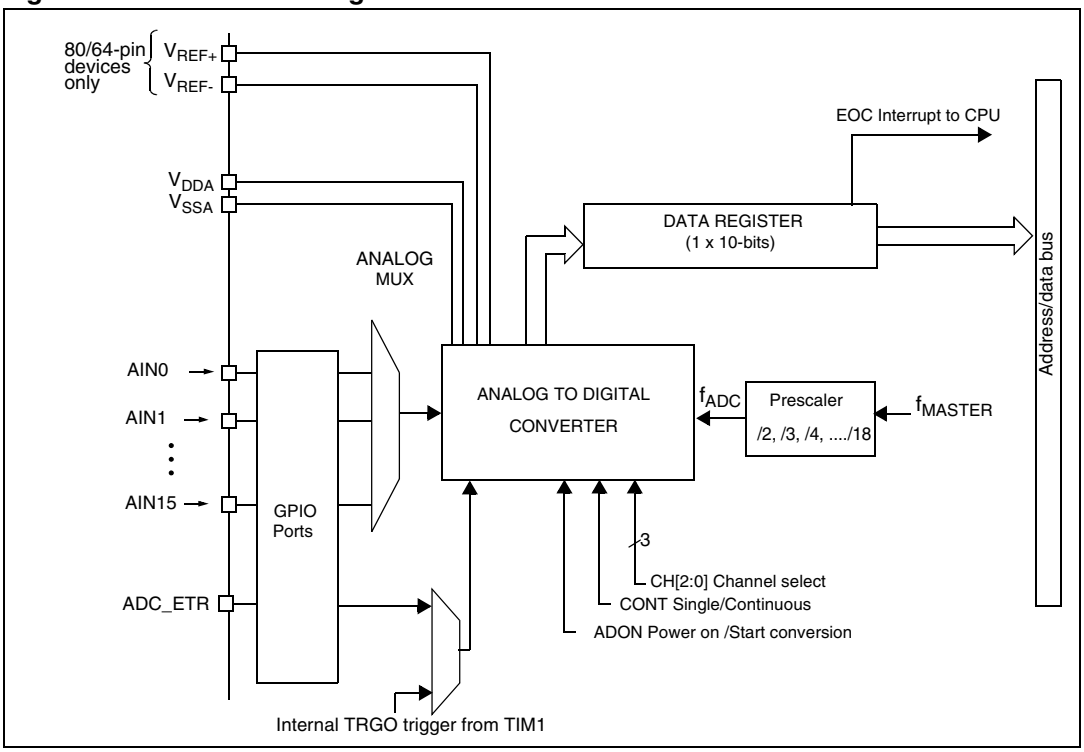


Figure 155. ADC2 block diagram



24.4 ADC pins

Table 66. ADC pins

Name	Signal type	Remarks
V_{DDA}	Input, Analog supply	Analog power supply. This input is bonded to V_{DD} in devices that have no external V_{DDA} pin.
V_{SSA}	Input, Analog supply ground	Ground for analog power supply. This input is bonded to V_{SS} in devices that have no external V_{SSA} pin.
V_{REF-}	Input, Analog Reference negative	The lower/negative reference voltage for the ADC, ranging from V_{SSA} to (V_{SSA} + 500 mV). This input is bonded to VSSA in devices that have no external VREF- pin (packages with 48 pins or less)
V_{REF+}	Input, Analog Reference positive	The higher/positive reference voltage for the ADC, ranging from 2.75 V to V_{DDA}. This input is bonded to V_{DDA} in devices that have no external VREF+ pin (packages with 48 pins or less)
AIN[15:0]	Analog input signals	Up to 16 analog input channels, which are converted by the ADC one at a time.
ADC_ETR	Digital input signals	External trigger.

24.5 ADC functional description

24.5.1 ADC on-off control

The ADC can be powered-on by setting the ADON bit in the ADC_CR1 register. When the ADON bit is set for the first time, it wakes up the ADC from power down mode. To start conversion, set the ADON bit in the ADC_CR1 register with a second write instruction.

At the end of conversion, the ADC remains powered on and you have to set the ADON bit only once to start the next conversion.

If the ADC is not used for a long time, it is recommended to switch it to power down mode to decrease power consumption. This is done by clearing the ADON bit.

When the ADC is powered on, the output stage of the selected channel is disabled, therefore it is recommended to select the channel first before powering-on the ADC.

24.5.2 ADC clock

The clock supplied to the ADC can by a prescaled f_{MASTER} clock. The prescaling factor of the clock depends on the SPSEL[2:0] bits in the ADC_CR1 register.

24.5.3 Channel selection

There are up to 16 external input channels. The number of external channels depends on the MCU package size.

If the channel selection is changed during a conversion, the current conversion is reset and a new start pulse is sent to the ADC.

24.5.4 Conversion modes

The ADC supports five conversion modes: single mode, continuous mode, buffered continuous mode, single scan mode, continuous scan mode.

Single mode

In Single conversion mode, the ADC does one conversion on the channel selected by the CH[3:0] bits in the ADC_CSR register. This mode is started by setting the ADON bit in the ADC_CR1 register, while the CONT bit is 0.

Once the conversion is complete, the converted data are stored in the ADC_DR register, the EOC (End of Conversion) flag is set and an interrupt is generated if the EOCIE bit is set.

Continuous and buffered continuous modes

In continuous conversion mode, the ADC starts another conversion as soon as it finishes one. This mode is started by setting the ADON bit in the ADC_CR1 register, while the CONT bit is set.

- If buffering is not enabled (DBUF bit = 0 in the ADC_CR3 register), the converted data is stored in the ADC_DR register and the EOC (End of Conversion) flag is set. An interrupt is generated if the EOCIE bit is set. Then a new conversion starts automatically.
- If buffering is enabled (DBUF bit =1) the data buffer is filled with the results of 8 or 10 consecutive conversions performed on a single channel. When the buffer is full, the EOC (End of Conversion) flag is set and an interrupt is generated if the EOCIE bit is set. Then a new set of 8 or 10 conversions starts automatically. The OVR flag is set if one of the data buffer registers is overwritten before it has been read (see *Section 24.5.5*).

To stop continuous conversion, reset the CONT bit to stop conversion or reset the ADON bit to power off the ADC.

Single scan mode

This mode is used to convert a sequence of analog channels from AIN0 to AINn where ‘n’ is the channel number defined by the CH[3:0] bits in the ADC_CSR register. During the scan conversion sequence the CH[3:0] bits are updated by hardware and contain the channel number currently being converted.

Single scan mode is started by setting the ADON bit while the SCAN bit is set and the CONT bit is cleared.

Note: When using scan mode, it is not possible to use channels AIN0 to AINn in output mode because the output stage of each channel is disabled when it is selected by the ADC multiplexer.

A single conversion is performed for each channel starting with AIN0 and the data is stored in the data buffer registers ADC_DBxR. When the last channel (channel ‘n’) has been converted, the EOC (End of Conversion) flag is set and an interrupt is generated if the EOCIE bit is set.

The converted values for each channel can be read from the data buffer registers. The OVR flag is set if one of the data buffer registers is overwritten before it has been read (see *Section 24.5.5*).

Do not clear the SCAN bit while the conversion sequence is in progress. Single scan mode can be stopped immediately by clearing the ADON bit.

To start a new SCAN conversion, clear the EOC bit and set the ADON bit in the ADC_CR1 register.

Continuous scan mode

This mode is like single scan mode except that each time the last channel has been converted, a new scan conversion from channel 0 to channel n starts automatically. The OVR flag is set if one of the data buffer registers is overwritten before it has been read (see *Section 24.5.5*).

Continuous scan mode is started by setting the ADON bit while the SCAN and CONT bits are set.

Do not clear the SCAN bit while scan conversion is in progress.

Continuous scan mode can be stopped immediately by clearing the ADON bit. Alternatively if the CONT bit is cleared while conversion is ongoing, conversion stops the next time the last channel has been converted.

Caution: In scan mode, do not use a bit manipulation instruction (BRES) to clear the EOC flag. This is because this performs a read-modify-write on the whole ADC_CSR register, reading the current channel number from the CH[3:0] register and writing it back, which changes the last channel number for the scan sequence.

The correct way to clear the EOC flag in continuous scan mode is to load a byte in the ADC_CSR register from a RAM variable, clearing the EOC flag and reloading the last channel number for the scan sequence

24.5.5 Overrun flag

The OVR error flag is set by hardware in buffered continuous mode, single scan or continuous scan modes. It indicates that one of the ten data buffer registers was overwritten by a new converted value before the previous value was read. In this case, it is recommended to start a new conversion.

Note: Setting the ADON bit automatically clears the OVR flag.

24.5.6 Analog watchdog

The analog watchdog is enabled for single conversion and non-buffered continuous conversion modes by setting the AWDEN bit in the ADC_CSR register.

The AWD analog watchdog flag is set if the analog voltage converted by the ADC is below a low threshold or above a high threshold as shown in *Figure 156*. These thresholds are programmed in the ADC_HTR and ADC_LTR 10-bit registers. An interrupt can be enabled by setting the AWDIE bit in the ADC_CSR register.

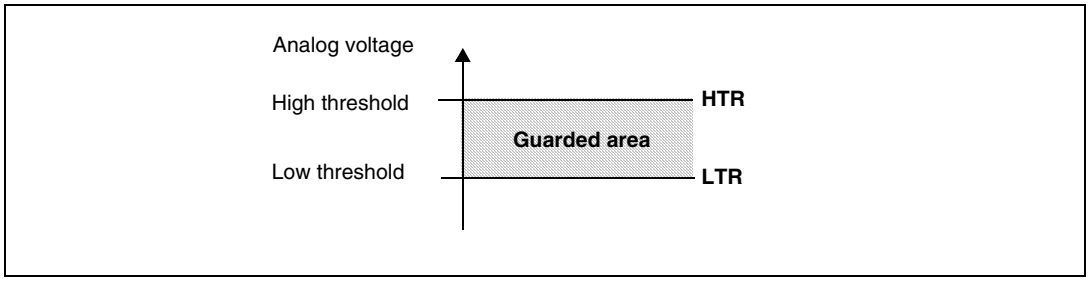
For Scan mode, the analog watchdog can be enabled on selected channels using the AWENx bits in the ADC_AWCRH and ADC_AWCRL registers. The watchdog status for each channel is obtained by reading the AWSx bits in the ADC_AWSRH and ADC_AWSRL registers. If any of the AWS flags are set, this also sets the AWD flag. Depending on the AWDIE interrupt enable bit, an interrupt is generated at the end of the SCAN sequence. The interrupt routine should then clear the AWS flag and the global AWD flag in the ADC_CSR register.

For Buffered continuous mode, the analog watchdog can be enabled on selected buffers, and is managed as described for scan mode, with the difference the buffers contain the results of continuous conversions performed on a single channel.

Refer to *Section 24.7* for more details on interrupts.

Note: To optimize analog watchdog interrupt latency in scan or buffered continuous mode, it recommended to use the last channels in the conversion sequence.

Figure 156. Analog watchdog guarded area



24.5.7 Conversion on external trigger

Conversion can be triggered by an rising edge event on the ADC_ETR pin or a TRGO event from a timer. Refer to the datasheet for details on the timer trigger, as this is product dependent). If the EXTTRIG control bit is set then either of the external events can be used to trigger a conversion. The EXTSEL[1:0] bits are used to select the two possible sources of events that can trigger conversion.

To use external trigger mode:

1. The ADC is in off state (ADON=0) and EOC bit is cleared.
2. Select trigger source (EXTSEL [1:0]).
3. Set external trigger mode EXTTRIG=1 using a BSET instruction in order not to change other bits in the register.
4. If the trigger source is in high state, this switches on the ADC. For this reason, test if ADC is switched off (ADON=0), then switch on ADC (ADON=1).
5. Wait for the stabilisation time (t_{STAB}). If an external trigger occurs before t_{STAB} elapses, the result will not be accurate.
6. Conversion starts when an external trigger event occurs.

Note: 1 If timer trigger mode is selected (timer event as trigger source, not external pin) it is recommended to start the timer only when the ADC is completely set - and stop the timer before the ADC is switched off.

2 External trigger mode must be disabled (EXTTRIG=0) before executing a HALT instruction.

24.5.8 Analog zooming

Analog zooming is supported in devices with external reference voltage pins (V_{REF+} and V_{REF-}). In analog zooming, the reference voltage is chosen to allow increased resolution in a reduced voltage range. Refer to the datasheet for details on the allowed reference voltage range.

24.5.9 Timing diagram

As shown in *Figure 157*, after ADC power on, the ADC needs a stabilization time t_{STAB} (equivalent to one conversion time t_{CONV}) before it starts converting accurately. For subsequent conversions there is no stabilization delay and ADON needs to be set only once. The ADC conversion time takes 14 clock cycles. After conversion the EOC flag is set and the 10-bit ADC Data register contains the result of the conversion.

Figure 157. Timing diagram in single mode (CONT = 0)

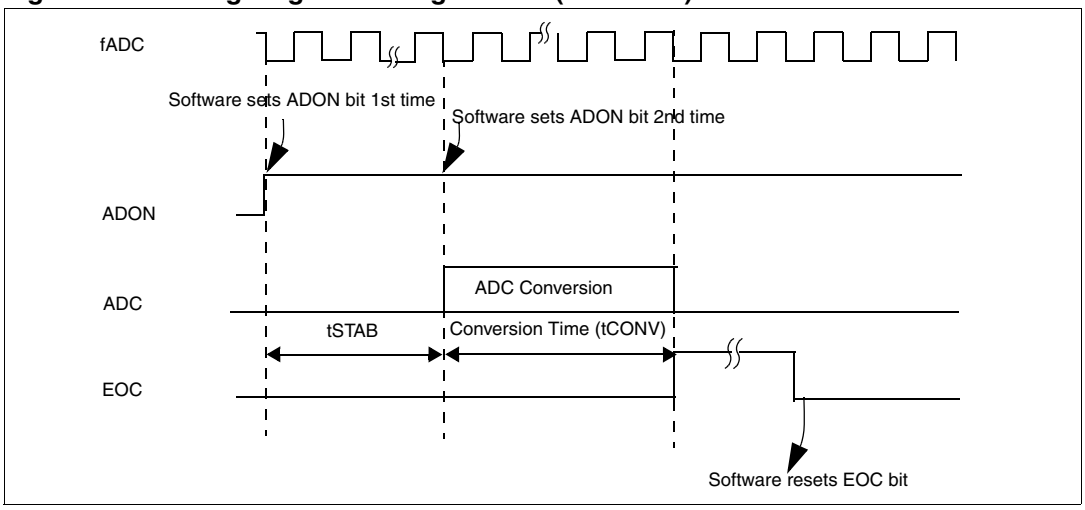
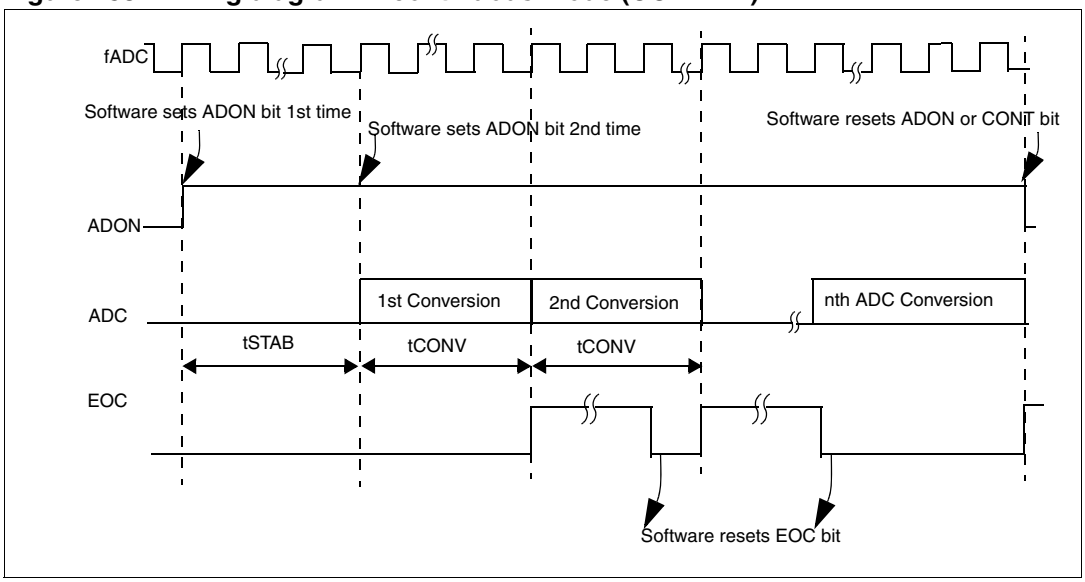


Figure 158. Timing diagram in continuous mode (CONT = 1)



24.6 ADC low power modes

Table 67. Low power modes

Mode	Description
WAIT	No effect on ADC
HALT/ Fast Active HALT/ Slow Active HALT	In devices with extended features, the ADC is automatically switched off before entering HALT/Active HALT mode. After waking up from HALT/Fast Active HALT or Slow Active HALT mode, the ADON bit must be set by software to power on the ADC, and a delay of 7 µs is needed before starting a new conversion.

The ADC does not have the capability to wake the device from Active Halt or Halt Mode.

24.7 ADC interrupts

The ADC interrupt control bits are summarized in *Table 68*, *Table 69* and *Table 70*

Table 68. ADC Interrupts in single and non-buffered continuous mode (ADC1 and ADC2)

Enable bits			Status flags			Exit from Wait	Exit from Halt
AWDENx	AWDIE	EOCIE	AWSx	AWDG	EOC		
Don't care	0	0	Don't care	Flag is set if the channel crosses the programmed thresholds.	Flag is set at the end of each conversion.	No	No
	0	1		Flag is set if the channel crosses the programmed thresholds.	Flag is set at the end of each conversion and an interrupt is generated.	Yes	No
	1	0		Flag is set if the channel crosses the programmed thresholds. An interrupt is generated but continuous conversion is not stopped.	Flag is set at the end of each conversion.	Yes	No
	1	1		Flag is set if the channel crosses the programmed thresholds. An interrupt is generated but continuous conversion is not stopped.	Flag is set at the end of each conversion and an interrupt is generated.	Yes	no

Table 69. ADC interrupts in buffered continuous mode (ADC1)

Enable bits			Status flags			Exit from Wait	Exit from Halt
AWENx	AWDIE	EOCIE	AWSx	AWD	EOC		
0	Don't care	0	0	0	The flag is set at the end of BSIZE conversions	No	No
0	Don't care	1	0		The flag is set at the end of BSIZE conversions and an interrupt is generated.	Yes	No
1	0	0	Flag is set if conversion on buffer "x" crosses the thresholds programmed in the ADC_HTR and ADC_LTR registers	The flag is set at the end of BSIZE conversions if at least one of the AWSx bits is set	The flag is set at the end of BSIZE conversions (Data Buffer Full)	No	No
1	1	0		The flag is set and an interrupt is generated at the end of BSIZE conversions if at least one of the AWSx bits is set. Continuous conversion is not stopped.		Yes	No
1	0	1		The flag is set at the end of BSIZE conversions if at least one of the AWSx bits is set	The flag is set at the end of BSIZE conversions and an interrupt is generated.	Yes	No
1	1	1		The flag is set immediately as soon as one of the AWSx bits is set. In interrupt is generated and continuous conversion is stopped.	The flag is set at the end of BSIZE conversions and an interrupt is generated.	Yes	No

Note: BSIZE = Data buffer size (8 or 10 depending on the product).

Table 70. ADC interrupts in scan mode (ADC1)

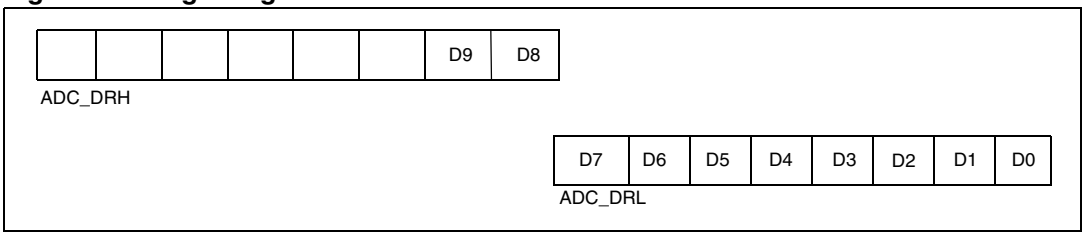
Control bits			Status bits			Exit from Wait	Exit from Halt
AWENx	AWDIE	EOCIE	AWSx	AWD	EOC		
0	Don't care	0	0	0	The flag is set at the end of the scan sequence	No	No
0	Don't care	1	0	0	The flag is set at the end of the scan sequence and an interrupt is generated.	Yes	No
1	0	0	Flag is set if conversion on channel "x" crosses the thresholds programmed in the ADC_HTR and ADC_LTR registers	The flag is set at the end of the scan sequence if at least one of the AWSx bits is set	The flag is set at the end of the scan sequence	No	No
1	1	0		The flag is set and an interrupt is generated at the end of the SCAN sequence if at least one of the AWSx bits is set. SCAN conversion is not stopped.	The flag is set to 1 at the end of the scan sequence	Yes	No
1	0	1		The flag is set at the end of the scan sequence if at least one of the AWSx bits is set	The flag is set to 1 at the end of the scan sequence and an interrupt is generated.	Yes	No
1	1	1		The flag is set immediately as soon as one of the AWSx bits is set. In interrupt is generated and scan conversion is stopped.	The flag is set at the end of the scan sequence and an interrupt is generated.	Yes	No

24.8 Data alignment

ALIGN bit in the ADC_CR2 register selects the alignment of data stored after conversion. Data can be aligned in the following ways.

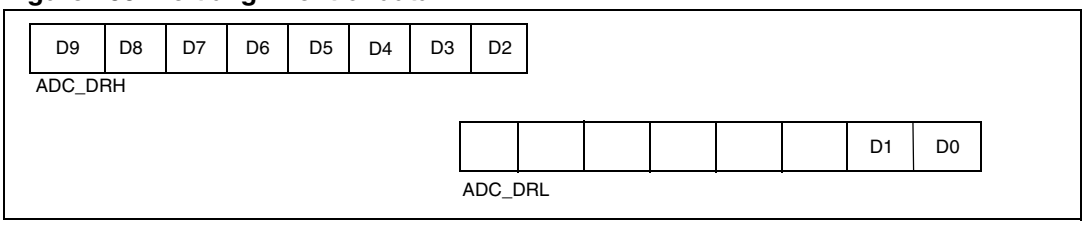
Right Alignment: 8 Least Significant bits are written in the ADC_DL register, then the remaining Most Significant bits are written in the ADC_DH register. The Least Significant Byte must be read first followed by the Most Significant Byte.

Figure 159. Right alignment of data



Left Alignment: 8 Most Significant bits are written in the ADC_DH register, then the remaining Least Significant bits are written in the ADC_DL register. The Most Significant Byte must be read first followed by the Least Significant Byte.

Figure 160. Left alignment of data



24.9 Reading the conversion result

The reading order of the ADC results from the buffer registers has no impact on data coherency. Consequently, the data may be incoherent and MSB/LSB can be overwritten by an incoming ADC conversion.

24.10 Schmitt trigger disable registers

The ADC_TDRH and ADC_TDRL registers are used to disable the Schmitt triggers available in the AIN analog input pins. Disabling the Schmitt trigger lowers the power consumption in the I/Os.

24.11 ADC registers

24.11.1 ADC data buffer register x high (ADC_DBxRH) (x=0..7 or 0..9)

Address offset: 0x00 + 2 * channel number

Reset value: 0x00

7	6	5	4	3	2	1	0
DBH[7:0]							
r	r	r	r	r	r	r	r

Note: Data buffer registers are not available for ADC2. The data buffer size and base address are device dependent and are specified in the corresponding datasheet. Note that the data buffer registers and the other ADC registers have different base addresses.

Bits 7:0 **DBH[7:0]** Data bits high

These bits are set/reset by hardware and are read only. When the ADC is in buffered continuous or scan mode, they contain the high part of the converted data. The data is in right-aligned or left-aligned format depending on the ALIGN bit.

Left Data Alignment

These bits contain the eight MSB bits of the converted data.

Right Data Alignment

These bits contain the (eight ADC data width) MSB bits of the converted data. Remaining bits are tied to zero.

See *Figure 159.*

24.11.2 ADC data buffer register x low (ADC_DBxRL) (x=or 0..7 or 0..9)

Address offset: 0x01 + 2 * channel number

Reset value: 0x00

7	6	5	4	3	2	1	0
DL[7:0]							
r	r	r	r	r	r	r	r

Note: Data buffer registers are not available for ADC2. The data buffer size and base address are device dependent and are specified in the corresponding datasheet. Note that the data buffer registers and the other ADC registers have different base addresses.

Bits 7:0 **DL[7:0]** Data bits low

These bits are set/reset by hardware and are read only. When the ADC is in buffered continuous or scan mode, they contain the low part of the A/D conversion result, in right-aligned or left-aligned format depending on the ALIGN bit.

Left Data Alignment

These bits contain the (eight ADC data width) LSB bits of the converted data. Remaining bits of the register are tied to zero.

See *Figure 160.*

Right Data Alignment

These bits contain the eight LSB bits of the converted data.

24.11.3 ADC control/status register (ADC_CSR)

Address offset: 0x00

Reset value: 0x00

7	6	5	4	3	2	1	0
EOC	AWD	EOCIE	AWDIE	CH[3:0]			
rw	rc_w0	rw	rw	rw	rw	rw	rw

Bit 7 **EOC**: End of conversion

This bit is set by hardware at the end of conversion. It is cleared by software by writing ‘0’.

0: Conversion is not complete

1: Conversion complete

Bit 6 **AWD**: Analog Watchdog flag

0: No analog watchdog event

1: An analog watchdog event occurred. In buffered continuous or scan mode you can read the ADC_AWSR register to determine the data buffer register related to the event. An interrupt request is generated if AWDIE=1.

Note: This bit is not available for ADC2

Bit 5 **EOCIE**: Interrupt enable for EOC

This bit is set and cleared by software. It enables the interrupt for End of Conversion.

0: EOC interrupt disabled

1: EOC interrupt enabled. An interrupt is generated when the EOC bit is set.

Bit 4 **AWDIE**: Analog watchdog interrupt enable

0: AWD interrupt disabled.

1: AWD interrupt enabled

Note: This bit is not available for ADC2

Bits 3:0 **CH[3:0]**: Channel selection bits

These bits are set and cleared by software. They select the input channel to be converted.

0000: Channel AIN0

0001: Channel AIN1

....

1111: Channel AIN15

24.11.4 ADC configuration register 1 (ADC_CR1)

Address offset: 0x01

Reset value: 0x00

7	6	5	4	3	2	1	0
Reserved	SPSEL[2:0]			Reserved		CONT	ADON
	rw	rw	rw			rw	rw

Bit 7 Reserved, always read as 0.

Bits 6:4 **SPSEL[2:0]**: Prescaler selection

These control bits are written by software to select the prescaler division factor.

000: $f_{ADC} = f_{MASTER}/2$
001: $f_{ADC} = f_{MASTER}/3$
010: $f_{ADC} = f_{MASTER}/4$
011: $f_{ADC} = f_{MASTER}/6$
100: $f_{ADC} = f_{MASTER}/8$
101: $f_{ADC} = f_{MASTER}/10$
110: $f_{ADC} = f_{MASTER}/12$
111: $f_{ADC} = f_{MASTER}/18$

See *Section 24.5.2 on page 410*.

Note: It is recommended to change the SPSEL bits when ADC is in power down. This is because internally there can be a glitch in the clock during this change. Otherwise the user is required to ignore the 1st converted result if the change is done when ADC is not in power down.

Bits 3:2 Reserved, always read as 0.

Bit 1 **CONT**: Continuous conversion

This bit is set and cleared by software. If set, conversion takes place continuously till this bit is reset by software.

0: Single conversion mode
1: Continuous conversion mode

Bit 0 **ADON**: A/D Converter on/off

This bit is set and reset by software. This bit must be written to wake up the ADC from power down mode and to trigger the start of conversion. If this bit holds a value of 0 and a 1 is written to it then it wakes the ADC from power down mode. Conversion starts when this bit holds a value of 1 and a 1 is written to it. As soon as the ADC is powered on, the output stage of the selected channel is disabled.

0: Disable ADC conversion/calibration and go to power down mode.
1: Enable ADC and to start conversion

Note: If any other bit in this register apart from ADON is changed at the same time, then conversion is not triggered. This is to prevent triggering an erroneous conversion.

24.11.5 ADC configuration register 2 (ADC_CR2)

Address offset: 0x02

Reset value: 0x00

7	6	5	4	3	2	1	0
Reserved	EXTTRIG	EXTSEL[1:0]		ALIGN	Reserved	SCAN	Reserved
	rw	rw	rw	rw		rw	

Bit 7 Reserved, must be kept cleared.

Bit 6 **EXTTRIG**: External trigger enable

This bit is set and cleared by software. It is used to enable an external trigger to trigger a conversion.

0: Conversion on external event disabled

1: Conversion on external event enabled

Note: To avoid a spurious trigger event, use the BSET instruction to set EXTTRIG without changing other bits in the register.

Bits 5:4 **EXTSEL[1:0]**: External event selection

The two bits are written by software. They select one of four types of event used to trigger the start of ADC conversion.

00: Internal TIM1 TRGO event

01: External interrupt on ADC_ETR pin

10: Reserved

11: Reserved

Bit 3 **ALIGN**: Data alignment

This bit is set and cleared by software.

0: Left alignment (the eight MSB bits are written in the ADC_DRH register then the remaining LSB bits are written in the ADC_DRL register). The reading order should be MSB first and then LSB.

1: Right alignment (eight LSB bits are written in the ADC_DRL register then the remaining MSB bits are written in the ADC_DH register). The reading order should be LSB first and then MSB.

Note: The ALIGN bit influences the ADC_DRH/ADC_DRL register reading order and not the reading order of the buffer registers.

Bit 2 Reserved, must be kept cleared.

Bit 1 **SCAN**: Scan mode enable

This bit is set and cleared by software.

0: Scan mode disabled

1: Scan mode enabled

Note: This bit is not available for ADC2

Bit 0 Reserved, must be kept cleared.

24.11.6 ADC configuration register 3 (ADC_CR3)

Address offset: 0x03

Reset value: 0x00

7	6	5	4	3	2	1	0
DBUF	OVR	Reserved					
rw	rc_w0						

Note: This register is not available for ADC2.

Bit 7 **DBUF**: Data buffer enable

This bit is set and cleared by software. It is used together with the CONT bit enable buffered continuous mode (DBUF=1, CONT=1). When DBUF is set, converted values are stored in the ADC_DBxRH and ADC_DBxRL registers instead of the ADC_DRH and ADC_DRL registers.

0: Data buffer disabled

1: Data buffer enabled

Bit 6 **OVR**: Overrun flag

This bit is set by hardware and cleared by software.

0: No overrun

1: An overrun was detected in the data buffer registers.

Refer to *Section 24.5.5 on page 412* for more details.

Bits 5:0 Reserved, must be kept cleared.

24.11.7 ADC data register high (ADC_DRH)

Address offset: 0x04

Reset value: undefined

7	6	5	4	3	2	1	0
DH[7:0]							
r	r	r	r	r	r	r	r

Bits 7:0 **DH[7:0]** Data bits high

These bits are set/reset by hardware and are read only. When the ADC is in single or non-buffered continuous mode, they contain the high part of the converted data, in right-aligned or left-aligned format depending on the ALIGN bit.

- **Left Data Alignment**

  These bits contain the 8 MSB bits of the converted data. The MSB must be read first before reading the LSB (see *Section 24.9: Reading the conversion result* and *Figure 160.*)

- **Right Data Alignment**

  These bits contain the (ADC data width - 8) MSB bits of the converted data. Remaining bits are tied to zero.

  See *Figure 159.*

24.11.8 ADC data register low (ADC_DRL)

Address offset: 0x05

Reset value: undefined

7	6	5	4	3	2	1	0
DL[7:0]							
r	r	r	r	r	r	r	r

Bits 7:0 **DL[7:0]** Data bits low

These bits are set/reset by hardware and are read only. When the ADC is in single or non-buffered continuous mode, they contain the low part of the A/D conversion result, in right-aligned or left-aligned format depending on the ALIGN bit.

- **Left Data Alignment**

  These bits contain the (ADC data width - 8) LSB bits of the converted data, remaining bits of the register are tied to zero.

  See *Figure 160.*

- **Right Data Alignment**

  These bits contain the 8 LSB bits of the converted data. The LSB must be read first before reading the MSB (see *Section 24.9: Reading the conversion result* and *Figure 159.*)

24.11.9 ADC Schmitt trigger disable register high (ADC_TDRH)

Address offset: 0x06

Reset value: 0x00

7	6	5	4	3	2	1	0
TD[15:8]							
rw	rw	rw	rw	rw	rw	rw	rw

Bits 7:0 **TD[15:8]** Schmitt trigger disable high

These bits are set and cleared by software. When a TDx bit is set, it disables the I/O port input Schmitt trigger of the corresponding ADC input channel x even if this channel is not being converted. This is needed to lower the static power consumption of the I/O port.

0: Schmitt trigger enabled

1: Schmitt trigger disabled

24.11.10 ADC Schmitt trigger disable register low (ADC_TDRL)

Address offset: 0x07

Reset value: 0x00

7	6	5	4	3	2	1	0
TD[7:0]							
rw	rw	rw	rw	rw	rw	rw	rw

Bits 7:0 **TD[7:0]** Schmitt trigger disable low

These bits are set and cleared by software. When a TDx bit is set, it disables the I/O port input Schmitt trigger of the corresponding ADC input channel x even if this channel is not being converted. This is needed to lower the static power consumption of the I/O port.

0: Schmitt trigger enabled

1: Schmitt trigger disabled

24.11.11 ADC high threshold register high (ADC_HTRH)

Address offset: 0x08

Reset value: 0xFF

7	6	5	4	3	2	1	0
HT[9:2]							
rw	rw	rw	rw	rw	rw	rw	rw

Note: This register is not available for ADC2.

Bits 7:0 **HT[9:2]** Analog Watchdog High Voltage threshold MSB
These bits are set and cleared by software. They define the MSB of the high threshold (V_{REFH}) for the Analog Watchdog.

24.11.12 ADC high threshold register low (ADC_HTRL)

Address offset: 0x09

Reset value: 0x03

7	6	5	4	3	2	1	0
Reserved						HT[1:0]	
						rw	rw

Note: This register is not available for ADC2.

Bits 7:2 Reserved, must be kept cleared.

Bits 1:0 **HT[1:0]** Analog watchdog high voltage threshold LSB
These bits are set and cleared by software. They define the LSB of the high threshold (V_{REFH}) for the Analog Watchdog.

24.11.13 ADC low threshold register high (ADC_LTRH)

Address offset: 0x0A

Reset value: 0x00

7	6	5	4	3	2	1	0
LT[9:2]							
rw	rw	rw	rw	rw	rw	rw	rw

Note: This register is not available for ADC2.

Bits 7:0 **LT[9:2]** Analog watchdog low voltage threshold MSB
These bits are set and cleared by software. They define the MSB of the low Threshold (V_{REFL}) for the Analog Watchdog.

24.11.14 ADC low threshold register low (ADC_LTRL)

Address offset: 0x0B

Reset value: 0x00

7	6	5	4	3	2	1	0
Reserved						LT[1:0]	
						rw	rw

Note: This register is not available for ADC2.

Bits 7:2 Reserved, must be kept cleared.

Bits 1:0 **LT[1:0]** Analog watchdog low voltage threshold LSB
These bits are set and cleared by software. They define the LSB of the low threshold (V_{REFL}) for the Analog Watchdog.

24.11.15 ADC watchdog status register high (ADC_AWSRH)

Address offset: 0x0C

Reset value: 0x00

7	6	5	4	3	2	1	0
Reserved						AWS[9:8]	
						rc_w0	rc_w0

Note: This register is not available for ADC2.

Bits 7:2 Reserved, must be kept cleared.

Bits 1:0 **AWS[9:8]** Analog watchdog status flags 9:8

These bits are set by hardware and cleared by software.

- In buffered continuous mode (DBUF=1, CONT=1) AWS flags behave as described in *Table 69.*
- In scan mode (SCAN=1) AWS flags behave as described in *Table 70.*

0: No analog watchdog event in data buffer register x.

1: Analog watchdog event occurred in data buffer register x.

24.11.16 ADC watchdog status register low (ADC_AWSRL)

Address offset: 0x0D

Reset value: 0x00

7	6	5	4	3	2	1	0
AWS[7:0]							
rc_w0	rc_w0	rc_w0	rc_w0	rc_w0	rc_w0	rc_w0	rc_w0

Note: This register is not available for ADC2.

Bits 7:0 **AWS[7:0]** Analog watchdog status flags 7:0

These bits are set by hardware and cleared by software.

- In buffered continuous mode (DBUF=1, CONT=1) AWS flags behave as described in *Table 69.*
- In scan mode (SCAN=1) AWS flags behave as described in *Table 70.*

0: No analog watchdog event in data buffer register x.

1: Analog watchdog event occurred in data buffer register x.

24.11.17 ADC watchdog control register high (ADC_AWCRH)

Address offset: 0x0E

Reset value: 0x00

7	6	5	4	3	2	1	0
Reserved						AWEN[9:8]	
						rw	rw

Note: This register is not available for ADC2.

Bits 7:2 Reserved, must be kept cleared.

Bits 1:0 **AWEN[9:8]** Analog watchdog enable bits 9:8

These bits are set and cleared by software.
In buffered continuous mode (DBUF=1, CONT=1) and in scan mode (SCAN=1) the AWENx bits enable the analog watchdog function for each of the 10 data buffer registers.
0: Analog watchdog disabled in data buffer register x.
1: Analog watchdog enabled in data buffer register x.

24.11.18 ADC watchdog control register low (ADC_AWCRL)

Address offset: 0x0F

Reset value: 0x00

7	6	5	4	3	2	1	0
AWEN[7:0]							
rw	rw	rw	rw	rw	rw	rw	rw

Note: This register is not available for ADC2.

Bits 7:0 **AWEN[7:0]** Analog watchdog enable bits 7:0

These bits are set and cleared by software.
In buffered continuous mode (DBUF=1, CONT=1) and in scan mode (SCAN=1) the AWENx bits enable the analog watchdog function for each of the 10 data buffer registers.
0: Analog watchdog disabled in data buffer register x.
1: Analog watchdog enabled in data buffer register x.

24.12 ADC register map and reset values

Table 71. ADC1 register map and reset values

Address offset	Register name	7	6	5	4	3	2	1	0
0x00	ADC1 _DB0RH Reset value	- 0	- 0	- 0	- 0	- 0	- 0	DATA9 0	DATA8 0
0x01	ADC1_DB0RL Reset value	DATA7 0	DATA6 0	DATA5 0	DATA4 0	DATA3 0	DATA2 0	DATA1 0	DATA0 0
. . .				. . .					
0x0E	ADC1 _DB7RH Reset value	- 0	- 0	- 0	- 0	- 0	- 0	DATA9 0	DATA8 0
0x0Fh	ADC1_DB7RL Reset value	DATA7 0	DATA6 0	DATA5 0	DATA4 0	DATA3 0	DATA2 0	DATA1 0	DATA0 0
0x10	ADC1 _DB8RH(1) Reset value	- 0	- 0	- 0	- 0	- 0	- 0	DATA9 0	DATA8 0
0x11	ADC1_DB8RL(1) Reset value	DATA7 0	DATA6 0	DATA5 0	DATA4 0	DATA3 0	DATA2 0	DATA1 0	DATA0 0
0x12	ADC1 _DB9RH(1) Reset value	- 0	- 0	- 0	- 0	- 0	- 0	DATA9 0	DATA8 0
0x13h	ADC1_DB9RL(1) Reset value	DATA7 0	DATA6 0	DATA5 0	DATA4 0	DATA3 0	DATA2 0	DATA1 0	DATA0 0
0x00	ADC1 _CSR Reset value	EOC 0	AWD 0	EOCIE 0	AWDIE 0	CH3 0	CH2 0	CH1 0	CH0 0
0x01	ADC1_CR1 Reset value	- 0	SPSEL2 0	SPSEL1 0	SPSEL0 0	- 0	- 0	CONT 0	ADON 0
0x02	ADC1_CR2 Reset value	- 0	EXTTRIG 0	EXTSEL1 0	EXTSEL0 0	ALIGN 0	- 0	SCAN 0	- 0
0x03	ADC1_CR3 Reset value	DBUF 0	OVR 0	- 0	- 0	- 0	- 0	- 0	- 0
0x04	ADC1_DRH Reset value	- x	- x	- x	- x	- x	- x	DATA9 x	DATA8 x
0x05	ADC1_DRL Reset value	DATA7 x	DATA6 x	DATA5 x	DATA4 x	DATA3 x	DATA2 x	DATA1 x	DATA0 x
0x06	ADC1_TDRH(2) Reset value	TD15 0	TD14 0	TD13 0	TD12 0	TD11 0	TD10 0	TD9 0	TD8 0
0x07	ADC1_TDRL Reset value	TD7 0	TD6 0	TD5 0	TD4 0	TD3 0	TD2 0	TD1 0	TD0 0
0x08	ADC1 _HTRH Reset value	HT9 1	HT8 1	HT7 1	HT6 1	HT5 1	HT4 1	HT3 1	HT2 1
0x09	ADC1_HTRL Reset value	- 0	- 0	- 0	- 0	- 0	- 0	HT1 1	HT0 1

Table 71. ADC1 register map and reset values (continued)

Address offset	Register name	7	6	5	4	3	2	1	0
0x0A	ADC1 _LTRH Reset value	LT9 0	LT8 0	LT7 0	LT6 0	LT5 0	LT4 0	LT3 0	LT2 0
0x0B	ADC1_LTRL Reset value	- 0	- 0	- 0	- 0	- 0	- 0	LT1 0	LT0 0
0x0C	ADC1 _AWSRH(2) Reset value	- 0	- 0	- 0	- 0	- 0	- 0	AWS9 0	AWS8 0
0x0D	ADC1_AWSRL Reset value	AWS7 0	AWS6 0	AWS5 0	AWS4 0	AWS3 0	AWS2 0	AWS1 0	AWS0 0
0x0E	ADC1 _AWCRH(2) Reset value	- 0	- 0	- 0	- 0	- 0	- 0	AWEN9 0	AWEN8 0
0x0F	ADC1_AWCRL Reset value	AWEN7 0	AWEN6 0	AWEN5 0	AWEN4 0	AWEN3 0	AWEN2 0	AWEN1 0	AWEN0 0

1. This register is reserved in devices with buffer size 8 x 10 bits.
2. This register is reserved in devices without ADC channels 8 and 9.

Table 72. ADC2 register map and reset values

Address offset	Register name	7	6	5	4	3	2	1	0
0x00	ADC2 _CSR Reset value	EOC 0	AWD 0	EOCIE 0	AWDIE 0	CH3 0	CH2 0	CH1 0	CH0 0
0x01	ADC2_CR1 Reset value	- 0	SPSEL2 0	SPSEL1 0	SPSEL0 0	- 0	- 0	CONT 0	ADON 0
0x02	ADC2_CR2 Reset value	- 0	EXTTRIG 0	EXTSEL1 0	EXTSEL0 0	ALIGN 0	- 0	- 0	- 0
0x03	ADC2_CR3 Reset value	DBUF 0	OVR 0	- 0	- 0	- 0	- 0	- 0	- 0
0x04	ADC2_DRH Reset value	- 0	- 0	- 0	- 0	- 0	- 0	DATA9 0	DATA8 0
0x05	ADC2_DRL Reset value	DATA7 0	DATA6 0	DATA5 0	DATA4 0	DATA3 0	DATA2 0	DATA1 0	DATA0 0
0x06	ADC2_TDRH Reset value	TD15 0	TD14 0	TD13 0	TD12 0	TD11 0	TD10 0	TD9 0	TD8 0
0x07	ADC2_TDRL Reset value	TD7 0	TD6 0	TD5 0	TD4 0	TD3 0	TD2 0	TD1 0	TD0 0