8 Option bytes

Option bytes contain configurations for device hardware features as well as the memory protection of the device. They are stored in a dedicated block of the memory. Except for the ROP (read-out protection) byte, each option byte has to be stored twice, in a regular form (OPTx) and a complemented one (NOPTx) for redundancy.

Option bytes can be modified in ICP mode (via SWIM) by accessing the EEPROM address shown in the table below.

Option bytes can also be modified 'on the fly' by the application in IAP mode, except the ROP option that can only be modified in ICP mode (via SWIM).

Refer to the STM8S Flash programming manual (PM0051) and STM8 SWIM communication protocol and debug module user manual (UM0470) for information on SWIM programming procedures.

Table 12: Option bytes

Addr.	Option name	Option byte no.	Option bits								Factory default setting
			7	6	5	4	3	2	1	0	
0x4800	Read-out protection (ROP)	OPT0	ROP [7:0]								00h
0x4801	User boot code(UBC)	OPT1	UBC [7:0]								00h
0x4802		NOPT1	NUBC [7:0]								FFh
0x4803	Alternate function remapping (AFR)	OPT2	AFR7	AFR6	AFR5	AFR4	AFR3	AFR2	AFR1	AFR0	00h
0x4804		NOPT2	NAFR7	NAFR6	NAFR5	NAFR4	NAFR3	NAFR2	NAFR1	NAFR0	FFh
0x4805h	Miscell. option	OPT3	Reserved			HSI TRIM	LSI_ EN	IWDG _HW	WWDG _HW	WWDG _HALT	00h
0x4806		NOPT3	Reserved			NHSI TRIM	NLSI_ EN	NIWDG _HW	NWWDG _HW	NWW G_HALT	FFh
0x4807	Clock option	OPT4	Reserved				EXT CLK	CKAWU SEL	PRS C1	PRS C0	00h
0x4808		NOPT4	Reserved				NEXT CLK	NCKA WUSEL	NPRSC1	NPR SC0	FFh
0x4809	HSE clock startup	OPT5	HSECNT [7:0]								00h
0x480A		NOPT5	NHSECNT [7:0]								FFh
0x480B	Reserved	OPT6	Reserved								00h

Addr.	Option name	Option byte no.	Option bits								Factory default setting
			7	6	5	4	3	2	1	0	
0x480C		NOPT6	Reserved								FFh
0x480D	Reserved	OPT7	Reserved								00h
0x480E		NOPT7	Reserved								FFh
0x487E	Bootloader	OPTBL	BL[7:0]								00h
0x487F		NOPTBL	NBL[7:0]								FFh

Table 13: Option byte description

Option byte no.	Description
OPT0	**ROP[7:0]** Memory readout protection (ROP) AAh: Enable readout protection (write access via SWIM protocol) *Note: Refer to the family reference manual (RM0016) section on Flash/EEPROM memory readout protection for details.*
OPT1	**UBC[7:0]** User boot code area 0x00: no UBC, no write-protection 0x01: Page 0 to 1 defined as UBC, memory write-protected 0x02: Page 0 to 3 defined as UBC, memory write-protected 0x03: Page 0 to 4 defined as UBC, memory write-protected ... 0x3E: Pages 0 to 63 defined as UBC, memory write-protected Other values: Reserved *Note: Refer to the family reference manual (RM0016) section on Flash write protection for more details.*
OPT2	**AFR[7:0]** Refer to following table for the alternate function remapping decriptions of bits [7:2].
OPT3	**HSITRIM**:High speed internal clock trimming register size 0: 3-bit trimming supported in CLK_HSITRIMR register 1: 4-bit trimming supported in CLK_HSITRIMR register

Option byte no.	Description
	LSI_EN:Low speed internal clock enable 0: LSI clock is not available as CPU clock source 1: LSI clock is available as CPU clock source
	IWDG_HW: Independent watchdog 0: IWDG Independent watchdog activated by software 1: IWDG Independent watchdog activated by hardware
	WWDG_HW: Window watchdog activation 0: WWDG window watchdog activated by software 1: WWDG window watchdog activated by hardware
	WWDG_HALT: Window watchdog reset on halt 0: No reset generated on halt if WWDG active 1: Reset generated on halt if WWDG active
OPT4	**EXTCLK**: External clock selection 0: External crystal connected to OSCIN/OSCOUT 1: External clock signal on OSCIN
	CKAWUSEL:Auto wake-up unit/clock 0: LSI clock source selected for AWU 1: HSE clock with prescaler selected as clock source for for AWU
	PRSC[1:0] AWU clock prescaler 0x: 16 MHz to 128 kHz prescaler 10: 8 MHz to 128 kHz prescaler 11: 4 MHz to 128 kHz prescaler
OPT5	**HSECNT[7:0]**:HSE crystal oscillator stabilization time 0x00: 2048 HSE cycles 0xB4: 128 HSE cycles 0xD2: 8 HSE cycles 0xE1: 0.5 HSE cycles

Option byte no.	Description
OPT6	Reserved
OPT7	Reserved
OPTBL	**BL[7:0]** Bootloader option byte For STM8S products, this option is checked by the boot ROM code after reset. Depending on the content of addresses 0x487E, 0x487F, and 0x8000 (reset vector), the CPU jumps to the bootloader or to the reset vector. Refer to the UM0560 (STM8L/S bootloader manual) for more details. For STM8L products, the bootloader option bytes are on addresses 0xXXXX and 0xXXXX+1 (2 bytes). These option bytes control whether the bootloader is active or not. For more details, refer to the UM0560 (STM8L/S bootloader manual) for more details.

Table 14: Description of alternate function remapping bits [7:0] of OPT2

Option byte no.	Description(1)
OPT2	**AFR7** Alternate function remapping option 7 0: AFR7 remapping option inactive: Default alternate function(2). 1: Port D4 alternate function = BEEP. **AFR6** Alternate function remapping option 6 0: AFR6 remapping option inactive: Default alternate functions(2). 1: Port B5 alternate function = I^2C_SDA; port B4 alternate function = I^2C_SCL. **AFR5** Alternate function remapping option 5 0: AFR5 remapping option inactive: Default alternate functions(2). 1: Port B3 alternate function = TIM1_ETR; port B2 alternate function = TIM1_NCC3; port B1 alternate function = TIM1_CH2N; port B0 alternate function = TIM1_CH1N. **AFR4** Alternate function remapping option 4 0: AFR4 remapping option inactive: Default alternate function(2). 1: Port D7 alternate function = TIM1_CH4. **AFR3** Alternate function remapping option 3 0: AFR3 remapping option inactive: Default alternate function(2). 1: Port D0 alternate function = TIM1_BKIN. **AFR2** Alternate function remapping option 2

Option byte no.	Description[1]
	0: AFR2 remapping option inactive: Default alternate function[2]. 1: Port D0 alternate function = CLK_CCO.Note: AFR2 option has priority over AFR3 if both are activated. **AFR1** Alternate function remapping option 1 0: AFR1 remapping option inactive: Default alternate functions[2]. 1: Port A3 alternate function = TIM3_CH1; port D2 alternate function TIM2_CH3. **AFR0** Alternate function remapping option 0 0: AFR0 remapping option inactive: Default alternate function[2]. 1: Port D3 alternate function = ADC_ETR.

(1) Do not use more than one remapping option in the same port.

(2) Refer to pinout description.