11 General purpose I/O ports (GPIO)

11.1 Introduction

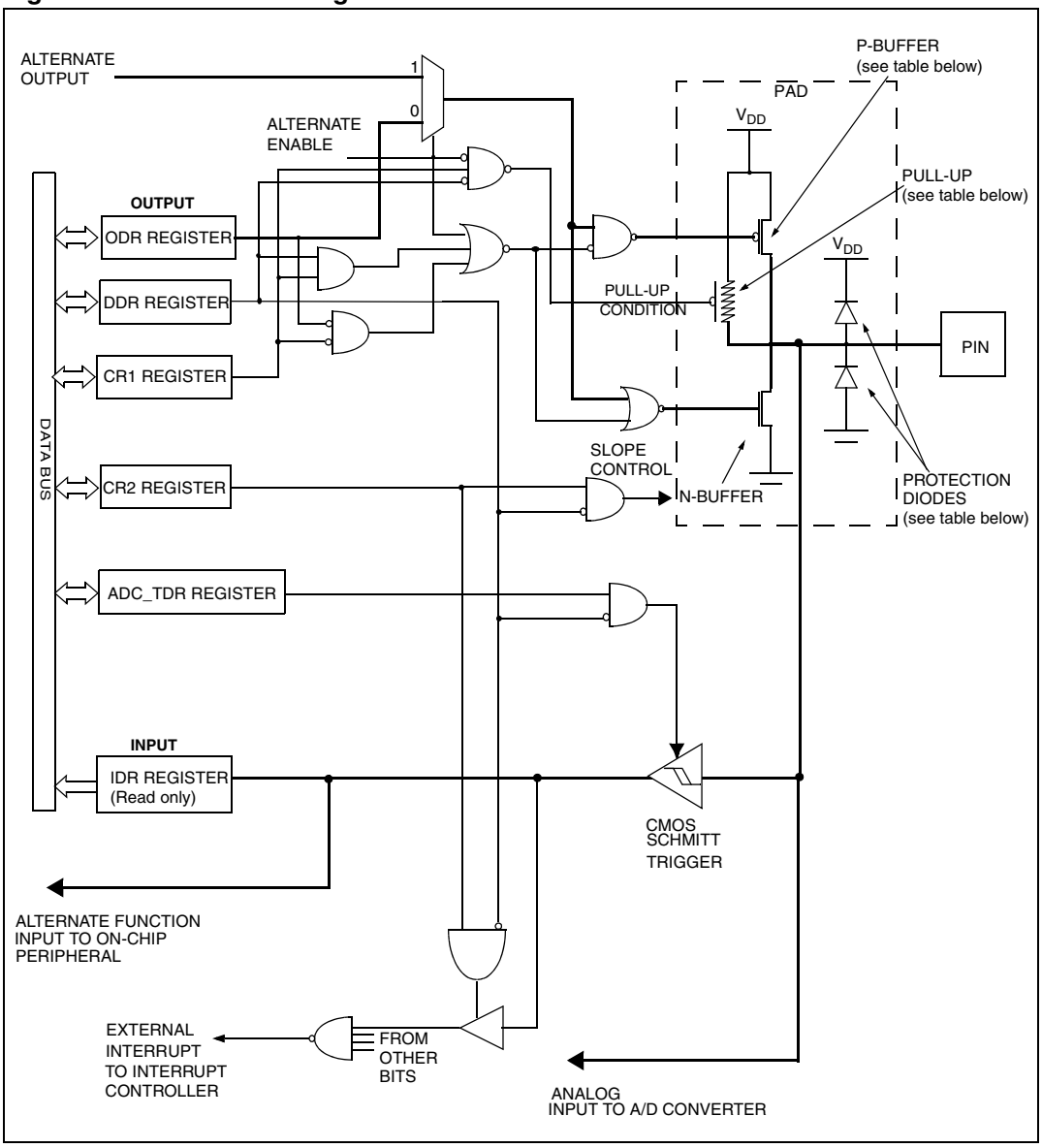
General purpose input/output ports are used for data transfers between the chip and the external world. An I/O port can contain up to eight pins. Each pin can be individually programmed as a digital input or digital output. In addition, some ports may have alternate functions like analog inputs, external interrupts, input/output for on-chip peripherals. Only one alternate function can be mapped to a pin at a time, the alternate function mapping is controlled by option byte. Refer to the datasheet for a description of the option bytes.

An output data register, Input pin register, data direction register, option register, and Configuration register are associated with each port. A particular port will behave as an input or output depending on the status of the data direction register of the port.

11.2 GPIO main features

- Port bits can be configured individually
- Selectable input modes: floating input or input with pull-up
- Selectable output modes: push-pull output or pseudo-open-drain.
- Separate registers for data input and output
- External interrupts can be enabled and disabled individually
- Output slope control for reduced EMC noise
- Alternate function I/Os for on-chip peripherals
- Input Schmitt trigger can be disabled on analog inputs for reduced power consumption
- Read-modify-write possible on data output latch
- 5 V-tolerant inputs
- I/O state guaranteed in voltage range 1.6 V to $V_{DDIOmax}$

Figure 21. GPIO block diagram



11.3 Port configuration and usage

An output data register (ODR), pin input register (IDR), data direction register (DDR) are always associated with each port.

The control register 1 (CR1) and control register 2 (CR2) allow input/output options. An I/O pin is programmed using the corresponding bits in the DDR, ODR, CR1 and CR2 registers.

Bit *n* in the registers corresponds to pin *n* of the Port.

The various configurations are summarized in *Table 17.*

Table 17. I/O port configuration summary

Mode	DDR bit	CR1 bit	CR2 bit	Function	Pull-up	P-buffer	Diodes	
							to V_{DD}	to V_{SS}
Input	0	0	0	Floating without interrupt	Off	Off	On	On
	0	1	0	Pull-up without interrupt	On			
	0	0	1	Floating with interrupt	Off			
	0	1	1	Pull-up with interrupt	On			
Output	1	0	0	Open drain output	Off	Off		
	1	1	0	Push pull output		On		
	1	x	1	Output speed limited to 10 MHz		Depends on CR1 bit		
	1	x	x	True open drain (on specific pins)	Not Implemented		Not implemented (see note)	

Note: The diode connected to V_{DD} is not implemented in true open drain pads. A local protection between the pad and V_{OL} is implemented to protect the device against positive stress.

Warning: On some packages, some ports must be considered as active even if they do not exist on the package. To avoid spurious effects, configure them as pull-up inputs without interrupt at startup, and keep them in this state when changing the port configuration. Refer to the datasheet for additional information.

11.3.1 Input modes

Clearing the DDRx bit selects input mode. In this mode, reading a IDR bit returns the digital value of the corresponding I/O pin.

Refer to *Section 11.7: Input mode details on page 103* for information on analog input, external interrupts and Schmitt trigger enable/disable.

As shown in *Table 17*, four different input modes can be theoretically be configured by software: floating without interrupt, floating with interrupt, pull-up without interrupt or pull-up with interrupt. However in practice, not all ports have external interrupt capability or pull-ups. You should refer to the datasheet pin-out description for details on the actual hardware capability of each port.

11.3.2 Output modes

Setting the DDRx bit selects output mode. In this mode, writing to the ODR bits applies a digital value to the I/O through the latch. Reading IDR bit returns the digital value from the corresponding I/O pin. Using the CR1, CR2 registers, different output modes can be configured by software: Push-pull output, Open-drain output.

Refer to *Section 11.8: Output mode details on page 104* for more information.

11.4 Reset configuration

At reset, all ports are input floating.

11.5 Unused I/O pins

Unused I/O pins must be connected to fixed voltage levels. Either connect a pull-up or pull-down to the unused I/O pins.

11.6 Low power modes

Table 18. Effect of low power modes on GPIO ports

Mode	Description
Wait	No effect on I/O ports. External interrupts cause the device to exit from Wait mode.
Halt	No effect on I/O ports. External interrupts cause the device to wakeup from Halt mode.

Note: If PA1/PA2 pins are used to connect an external oscillator, to ensure a lowest power consumption in Halt mode, PA1 and PA2 must be configured as input pull-up.

11.7 Input mode details

11.7.1 Alternate function input

Some I/Os can be used as alternate function input. For example as the port may be used as the input capture input to a timer. Alternate function inputs are not selected automatically, you select them by writing to a control bit in the registers of the corresponding peripheral. For Alternate Function input, you should select floating or pull-up input configuration in the DDR and CR1 registers.

11.7.2 Interrupt capability

You can configure an I/O as an input with interrupt by setting the CR2x bit while the I/O is in input mode. In this configuration, a signal edge or level input on the I/O generates an interrupt request.

Falling or rising edge sensitivity is programmed independently for each interrupt vector in the EXTI_CR[2:1] registers.

External interrupt capability is only available if the port is configured in input mode.

Interrupt masking

Interrupts can be enabled/disabled individually by programming the corresponding bit in the configuration register (Px_CR2). At reset the interrupts are disabled.

11.7.3 Analog channels

Analog channels of the I/O port can be selected by the ADC peripheral. As mentioned in the next section, the input Schmitt trigger should be disabled in the ADC_TDR register when using the analog channels.

Table 19. Recommended and non-recommended configurations for analog input

DDR	CR1	CR2	ADC_TDR	Configuration	Comments
0	0	0	1	Floating Input without interrupt, Schmitt trigger disabled	Recommended analog input configuration
0	1	x	x	Input with pull-up enabled	Not recommended for analog input, if analog voltage is present, these configurations cause excess current flow on the input pin.
1	0	x	x	Output	
1	1	x	x	Output	

11.7.4 Schmitt trigger

An internal input Schmitt trigger is included in some I/Os. The Schmitt trigger can be enabled/disabled using the ADC_TDR Schmitt trigger disable register.

11.8 Output mode details

11.8.1 Alternate function output

Alternate function outputs provide a direct path from a peripheral to an output or to an I/O pad, taking precedence over the port bit in the data output latch register (Px_ODR) and forcing the Px_DDR corresponding bit to 1.

An alternate function output can be push-pull or pseudo-open drain depending on the peripheral and Control register 1 (Px_CR1) and slope can be controlled depending on the Control register 2 (Px_CR2) values.

Examples:

SPI output pins must be set-up as push-pull, fast slope for optimal operation. USART_Tx can be configured either in push-pull or open drain with an external pull-up in order to implement multi slave configuration.

11.8.2 Slope control

The output frequency can be controlled by software using the CR2 bit. Setting the CR bit selects 10 MHz output frequency. This feature can be applied in either open drain or push-Pull output mode on I/O ports of output type O3 or O4. Refer to the pin description table for the specific output type information for each port.

11.9 GPIO registers

The bit of each port register drives the corresponding pin of the port.

11.9.1 Port x output data register (Px_ODR)

Address offset: 0x00

Reset value: 0x00

7	6	5	4	3	2	1	0
ODR7	ODR6	ODR5	ODR4	ODR3	ODR2	ODR1	ODR0
rw	rw	rw	rw	rw	rw	rw	rw

Bits 7:0 **ODR[7:0]**: Output data register bits

Writing to the ODR register when in output mode applies a digital value to the I/O through the latch. Reading the ODR returns the previously latched value in the register.

In Input mode, writing in the ODR register, latches the value in the register but does not change the pin state. The ODR register is always cleared after reset. Bit read-modify-write instructions (BSET, BRST) can be used on the DR register to drive an individual pin without affecting the others.

11.9.2 Port x pin input register (Px_IDR)

Address offset: 0x01

Reset value: 0x00

7	6	5	4	3	2	1	0
IDR7	IDR6	IDR5	IDR4	IDR3	IDR2	IDR1	IDR0
r	r	r	r	r	r	r	r

Bits 7:0 **IDR[7:0]**: Pin input values

The pin register can be used to read the pin value irrespective of whether port is in input or output mode. This register is read-only.

0: Low logic level

1: High logic level

11.9.3 Port x data direction register (Px_DDR)

Address offset: 0x02

Reset value: 0x00

7	6	5	4	3	2	1	0
DDR7	DDR6	DDR5	DDR4	DDR3	DDR2	DDR1	DDR0
rw	rw	rw	rw	rw	rw	rw	rw

Bits 7:0 **DDR[7:0]**: Data direction bits

These bits are set and cleared by software to select input or output mode for a particular pin of a port.

0: Input mode

1: Output mode

11.9.4 Port x control register 1 (Px_CR1)

Address offset: 0x03

Reset value: 0x00

7	6	5	4	3	2	1	0
C17	C16	C15	C14	C13	C12	C11	C10
rw	rw	rw	rw	rw	rw	rw	rw

Bits 7:0 **C1[7:0]**: *Control bits*

These bits are set and cleared by software. They select different functions in input mode and output mode *see Table 17 on page 101.*

- **In input mode (DDR = 0):**

0: Floating input

1: Input with pull-up

- **In output mode (DDR = 1):**

0: Pseudo open drain

1: Push-pull, slope control for the output depends on the corresponding CR2 bit

Note: This bit has no effect on true open drain ports (refer to pin marked "T" in datasheet pin description table).

11.9.5 Port x control register 2 (Px_CR2)

Address offset: 0x04

Reset value: 0x00

7	6	5	4	3	2	1	0
C27	C26	C25	C24	C23	C22	C21	C20
rw	rw	rw	rw	rw	rw	rw	rw

Bits 7:0 **C2[7:0]**: Control bits

These bits are set and cleared by software. They select different functions in input mode and output mode. In input mode, the CR2 bit enables the interrupt capability if available. If the I/O does not have interrupt capability, setting the CR2 bit has no effect. In output mode, setting the bit increases the speed of the I/O. This applies to ports with O3 and O4 output types (see pin description table).

- **In input mode (DDR = 0):**

0: External interrupt disabled

1: External interrupt enabled

- **In output mode (DDR = 1):**

0: Output speed up to 2 MHz

1: Output speed up to 10 MHz

11.9.6 GPIO register map and reset values

Each GPIO port has five registers mapped as shown in *Table 20*. Refer to the register map in the corresponding datasheet for the base address for each port.

Note: At reset, all ports are input floating. Exceptions are indicated in the pin description table of the corresponding datasheet.

Table 20. GPIO register map

Address offset	Register name	7	6	5	4	3	2	1	0
0x00	Px_ODR	ODR7 0	ODR6 0	ODR5 0	ODR4 0	ODR3 0	ODR2 0	ODR1 0	ODR0 0
0x01	Px_IDR	IDR7 0	IDR6 0	IDR5 0	IDR4 0	IDR3 0	IDR2 0	IDR1 0	IDR0 0
0x02	Px_DDR	DDR7 0	DDR6 0	DDR5 0	DDR4 0	DDR3 0	DDR2 0	DDR1 0	DDR0 0
0x03	Px_CR1	C17 0	C16 0	C15 0	C14 0	C13 0	C12 0	C11 0	C10 0
0x04	Px_CR2	C27 0	C26 0	C25 0	C24 0	C23 0	C22 0	C21 0	C20 0