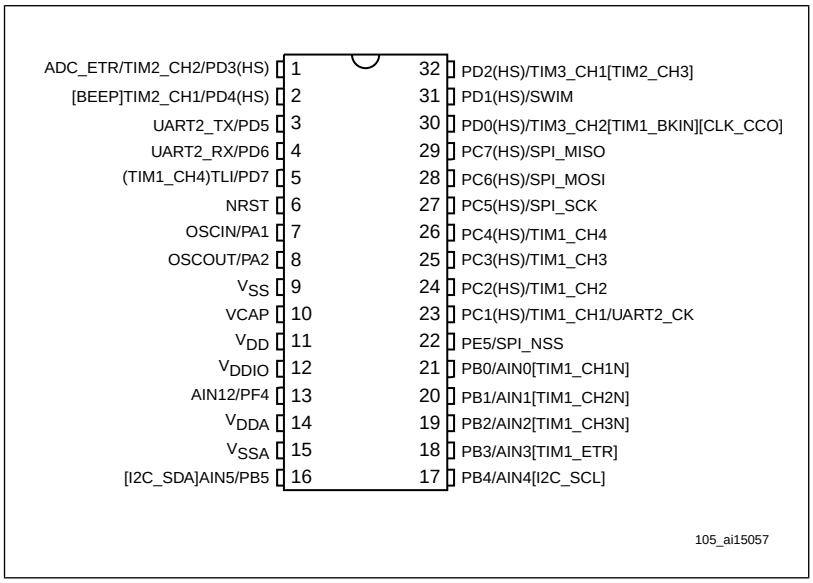
Figure 6: SDIP 32-pin pinout



1. (HS) high sink capability.
2. (T) True open drain (P-buffer and protection diode to V_{DD} not implemented).
3. [ ] alternate function remapping option (If the same alternate function is shown twice, it indicates an exclusive choice not a duplication of the function).

Table 6: Pin description for STM8S105 microcontrollers

Pin number				Pin name	Type	Input			Output				Main function (after reset)	Default alternate function	Alternate function after remap [option bit]
LQFP48	LQFP44	LQFP32/ VFQFPN32/ UFQFPN32	SDIP32			floating	wpu	Ext. interrupt	High sink	Speed	OD	PP			
1	1	1	6	NRST	I/O		**X**						Reset		
2	2	2	7	PA1/ OSC IN	I/O	**X**	X			O1	X	X	**Port A1**	Resonator/ crystal in	
3	3	3	8	PA2/ OSC OUT	I/O	**X**	X	X		O1	X	X	**Port A2**	Resonator/ crystal out	
4	4	-	-	V_{SSIO_1}	S								I/O ground		
5	5	4	9	V_{SS}	S								Digital ground		
6	6	5	10	VCAP	S								1.8 V regulator capacitor		
7	7	6	11	V_{DD}	S								Digital power supply		
8	8	7	12	V_{DDIO_1}	S								I/O power supply		

Pin number				Pin name	Type	Input			Output				Main function (after reset)	Default alternate function	Alternate function after remap [option bit]
LQFP48	LQFP44	LQFP32/ VFQFPN32/ UFQFPN32	SDIP32			floating	wpu	Ext. interrupt	High sink	Speed	OD	PP			
9	-	-	-	PA3/ TIM2 _CH3 [TIM3 _CH1]	I/O	**X**	X	X		O1	X	X	**Port A3**	Timer 2 - channel 3	TIM3_ CH1 [AFR1]
10	9	-	-	PA4	I/O	**X**	X	X	HS	O3	X	X	**Port A4**		
11	10	-	-	PA5	I/O	**X**	X	X	HS	O3	X	X	**Port A5**		
12	11	-	-	PA6	I/O	**X**	X	X	HS	O3	X	X	**Port A6**		
-	-	8	13	PF4/ AIN12	I/O	**X**	X			O1	X	X	**Port F4**	Analog input 12 *(1)*	
13	12	9	14	V_{DDA}	S								Analog power supply		
14	13	10	15	V_{SSA}	S								Analog ground		
15	14	-	-	PB7/ AIN7	I/O	**X**	X	X		O1	X	X	**Port B7**	Analog input 7	
16	15	-	-	PB6/ AIN6	I/O	**X**	X	X		O1	X	X	**Port B6**	Analog input 6	
17	16	11	16	PB5/ AIN5 [I^2C_ SDA]	I/O	**X**	X	X		O1	X	X	**Port B5**	Analog input 5	I^2C_SDA [AFR6]
18	17	12	17	PB4/ AIN4 [I^2C_ SCL]	I/O	**X**	X	X		O1	X	X	**Port B4**	Analog input 4	I^2C_SCL [AFR6]
19	18	13	18	PB3/ AIN3 [TIM1_ ETR]	I/O	**X**	X	X		O1	X	X	**Port B3**	Analog input 3	TIM1_ ETR [AFR5]
20	19	14	19	PB2/ AIN2 [TIM1_ CH3N]	I/O	**X**	X	X		O1	X	X	**Port B2**	Analog input 2	TIM1_ CH3N [AFR5]
21	20	15	20	PB1/ AIN1 [TIM1_ CH2N]	I/O	**X**	X	X		O1	X	X	**Port B1**	Analog input 1	TIM1_ CH2N [AFR5]
22	21	16	21	PB0/ AIN0 [TIM1_ CH1N]	I/O	**X**	X	X		O1	X	X	**Port B0**	Analog input 0	TIM1_ CH1N [AFR5]
23	-	-	-	PE7/ AIN8	I/O	**X**	X	X		O1	X	X	**Port E7**	Analog input 8	

Pin number				Pin name	Type	Input			Output				Main function (after reset)	Default alternate function	Alternate function after remap [option bit]
LQFP48	LQFP44	LQFP32/ VFQFPN32/ UFQFPN32	SDIP32			floating	wpu	Ext. interrupt	High sink	Speed	OD	PP			
24	22	-	-	PE6/ AIN9	I/O	**X**	X	X		O1	X	X	**Port E6**	Analog input 9 (2)	
25	23	17	22	PE5/SPI_ NSS	I/O	**X**	X	X		O1	X	X	**Port E5**	SPI master/slave select	
26	24	18	23	PC1/ TIM1_ CH1/ UART2_CK	I/O	**X**	X	X	HS	O3	X	X	**Port C1**	Timer 1 - channel 1/ UART2 synchronous clock	
27	25	19	24	PC2/ TIM1_ CH2	I/O	**X**	X	X	HS	O3	X	X	**Port C2**	Timer 1- channel 2	
28	26	20	25	PC3/ TIM1_ CH3	I/O	**X**	X	X	HS	O3	X	X	**Port C3**	Timer 1 - channel 3	
29	-	21	26	PC4/ TIM1_ CH4	I/O	**X**	X	X	HS	O3	X	X	**Port C4**	Timer 1 - channel 4	
30	27	22	27	PC5/ SPI_ SCK	I/O	**X**	X	X	HS	O3	X	X	**Port C5**	SPI clock	
31	28	-	-	V_{SSIO_2}	S								I/O ground		
32	29	-	-	V_{DDIO_2}	S								I/O power supply		
33	30	23	28	PC6/ SPI_ MOSI	I/O	**X**	X	X	HS	O3	X	X	**Port C6**	SPI master out/slave in	
34	31	24	29	PC7/ SPI_ MISO	I/O	**X**	X	X	HS	O3	X	X	**Port C7**	SPI master in/ slave out	
35	32	-	-	PG0	I/O	**X**	X			O1	X	X	**Port G0**		
36	33	-	-	PG1	I/O	**X**	X			O1	X	X	**Port G1**		
37	-	-	-	PE3/ TIM1_ BKIN	I/O	**X**	X	X		O1	X	X	**Port E3**	Timer 1 - break input	
38	34	-	-	PE2/ I^2C_ SDA	I/O	**X**	X	X		O1	T (3)		**Port E2**	I^2C data	
39	35	-	-	PE1/ I^2C_ SCL	I/O	**X**	X	X		O1	T (3)		**Port E1**	I^2C clock	
40	36	-	-	PE0/ CLK_ CCO	I/O	**X**	X	X	HS	O3	X	X	**Port E0**	Configurable clock output	

Pin number				Pin name	Type	Input			Output				Main function (after reset)	Default alternate function	Alternate function after remap [option bit]
LQFP48	LQFP44	LQFP32/ VFQFPN32/ UFQFPN32	SDIP32			floating	wpu	Ext. interrupt	High sink	Speed	OD	PP			
41	37	25	30	PD0/ TIM3_ CH2 [TIM1_ BKIN] [CLK_ CCO]	I/O	**X**	X	X	HS	O3	X	X	**Port D0**	Timer 3 - channel 2	TIM1_ BKIN [AFR3]/ CLK_ CCO [AFR2]
42	38	26	31	PD1/ SWIM	I/O	**X**	X	X	HS	O4	X	X	**Port D1**	SWIM data interface	
43	39	27	32	PD2/ TIM3_ CH1 [TIM2_ CH3]	I/O	**X**	X	X	HS	O3	X	X	**Port D2**	Timer 3 - channel 1	TIM2_CH3 [AFR1]
44	40	28	1	PD3/ TIM2_ CH2 [ADC_ ETR]	I/O	**X**	X	X	HS	O3	X	X	**Port D3**	Timer 2 - channel 2	ADC_ ETR [AFR0]
45	41	29	2	PD4/ TIM2_ CH1 [BEEP]	I/O	**X**	X	X	HS	O3	X	X	**Port D4**	Timer 2 - channel 1	BEEP output [AFR7]
46	42	30	3	PD5/ UART2_ TX	I/O	**X**	X	X		O1	X	X	**Port D5**	UART2 data transmit	
47	43	31	4	PD6/ UART2_ RX	I/O	**X**	X	X		O1	X	X	**Port D6**	UART2 data receive	
48	44	32	5	PD7/ TLI [TIM1_ CH4]	I/O	**X**	X	X		O1	X	X	**Port D7**	Top level interrupt	TIM1_ CH4 [AFR4]

(1) AIN12 is not selectable in ADC scan mode or with analog watchdog.

(2) In 44-pin package, AIN9 cannot be used by ADC scan mode.

(3) In the open-drain output column, 'T' defines a true open-drain I/O (P-buffer and protection diode to V_{DD} are not implemented).

5.1.1 Alternate function remapping

As shown in the rightmost column of the pin description table, some alternate functions can be remapped at different I/O ports by programming one of eight AFR (alternate function remap) option bits. When the remapping option is active, the default alternate function is no longer available.

To use an alternate function, the corresponding peripheral must be enabled in the peripheral registers.

Alternate function remapping does not effect GPIO capabilities of the I/O ports (see the GPIO section of the family reference manual, RM0016).