7 Interrupt vector mapping

Table 11: Interrupt mapping

IRQ no.	Source block	Description	Wakeup from halt mode	Wakeup from active-halt mode	Vector address
	RESET	Reset	Yes	Yes	0x00 8000
	TRAP	Software interrupt	-	-	0x00 8004
0	TLI	External top level interrupt	-	-	0x00 8008
1	AWU	Auto wake up from halt	-	Yes	0x00 800C
2	CLK	Clock controller	-	-	0x00 8010
3	EXTI0	Port A external interrupts	Yes(1)	Yes(1)	0x00 8014
4	EXTI1	Port B external interrupts	Yes	Yes	0x00 8018
5	EXTI2	Port C external interrupts	Yes	Yes	0x00 801C
6	EXTI3	Port D external interrupts	Yes	Yes	0x00 8020
7	EXTI4	Port E external interrupts	Yes	Yes	0x00 8024
8					0x00 8028
9		Reserved	-	-	0x00 802C
10	SPI	End of transfer	Yes	Yes	0x00 8030
11	TIM1	TIM1 update/ overflow/ underflow/ trigger/ break	-	-	0x00 8034
12	TIM1	TIM1 capture/ compare	-	-	0x00 8038
13	TIM	TIM update/ overflow	-	-	0x00 803C
14	TIM	TIM capture/ compare	-	-	0x00 8040

IRQ no.	Source block	Description	Wakeup from halt mode	Wakeup from active-halt mode	Vector address
15	TIM3	Update/ overflow	-	-	0x00 8044
16	TIM3	Capture/ compare	-	-	0x00 8048
17		Reserved	-	-	0x00 804C
18		Reserved	-	-	0x00 8050
19	I^2C	I^2C interrupt	Yes	Yes	0x00 8054
20	UART2	Tx complete	-	-	0x00 8058
21	UART2	Receive register DATA FULL	-	-	0x00 805C
22	ADC1	ADC1 end of conversion/ analog watchdog interrupt	-	-	0x00 8060
23	TIM	TIM update/ overflow	-	-	0x00 8064
24	Flash	EOP/ WR_PG_DIS	-	-	0x00 8068
Reserved					0x00 806C to 0x00 807C

(1) Except PA1