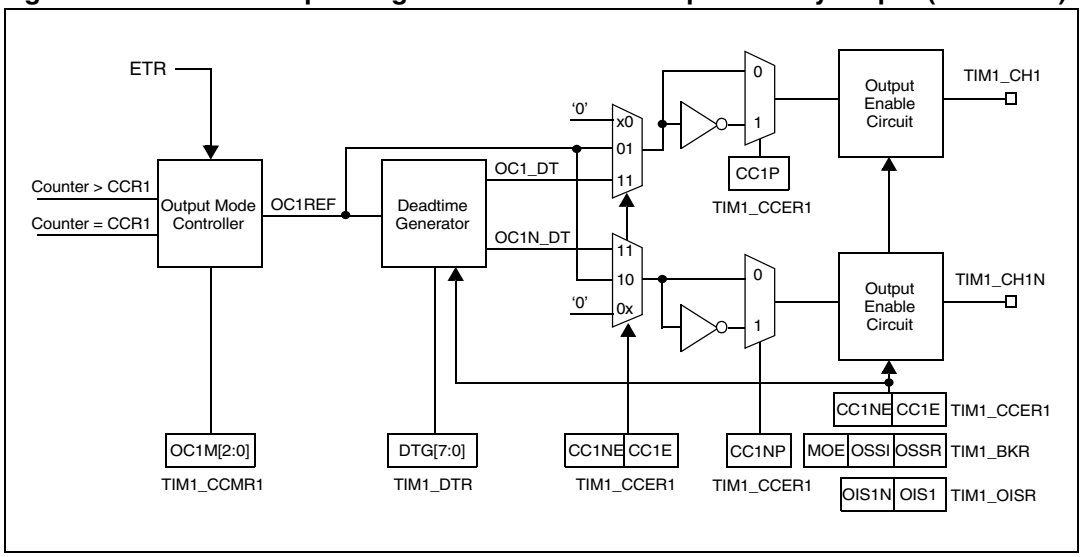
Figure 65. Detailed output stage of channel with complementary output (channel 1)



17.5.5 Forced output mode

In output mode (CC*i*S bits = 00 in the TIM1_CCMR*i* registers), each output compare signal can be forced to high or low level directly by software, independently of any comparison between the output compare register and the counter.

To force an output compare signal to its active level, write 101 in the OC*i*M bits in the corresponding TIM1_CCMR*i* registers. OC*i*REF is forced high (OC*i*REF is always active high) and the OC*i* output is forced high or low depending on the CC*i*P polarity bits.

For example, if CC*i*P = 0 (OC*i* active high) => OC*i* is forced high.

The OC*i*REF signal can be forced low by writing the OC*i*M bits to 100 in the TIMx_CCMRx registers.

Nevertheless, the comparison between the TIM1_CCR*i* shadow registers and the counter is still performed and allows the flag to be set. Interrupt requests can be sent accordingly. This is described in the output compare mode section below.

17.5.6 Output compare mode

This function is used to control an output waveform or indicate when a period of time has elapsed.

When a match is found between the capture/compare register and the counter:

- Depending on the output compare mode, the corresponding OC*i* output pin:
  - Keeps its level (OC*i*M = 000),
  - Is set active (OC*i*M = 001),
  - Is set inactive (OC*i*M = 010)
  - Toggles (OC*i*M = 011)
- A flag is set in the interrupt status register (CC*i*IF bits in the TIM1_SR1 register).
- An interrupt is generated if the corresponding interrupt mask is set (CC*i*IE bits in the TIM1_IER register).