17.5.3 Input capture mode

In input capture mode, the capture/compare registers (TIM1_CCR*i*) are used to latch the value of the counter after a transition detected on the corresponding IC*i* signal. When a capture occurs, the corresponding CC*i*IF flag (TIM1_SR1 register) is set.

An interrupt can be sent if it is enabled, by setting the CC*i*IE bits in the TIM1_IER register. If a capture occurs while the CC*i*IF flag is already high, the over-capture flag CC*i*OF (TIM1_SR2 register) is set. CC*i*IF can be cleared by software by writing it to 0 or by reading the captured data stored in the TIMx_CCR*i*L registers. CC*i*OF is cleared by writing it to 0.

Procedure

The following procedure shows how to capture the counter value in TIM1_CCR1, for example, when TI1 input rises.

1. Select the active input: For example, to link the TIM1_CCR1 register to the TI1 input, write the CC1S bits to 01 in the TIM1_CCMR1 register. This configures the channel in input mode and the TIM1_CCR1 register becomes read-only.
2. Program the required input filter duration for the signal to be connected to the timer. This is done for each TI*i* input using the IC*i*F bits in the TIM1_CCMR*i* registers. For example, if the input signal is unstable for up to five t_{MASTER} cycles when it toggles, the filter duration must be performed for longer than five clock cycles. The filter bits allow a duration of eight cycles to be selected by writing them to 0011 in the TIMx_CCMR1 register. With this filter setting, a transition on TI1 is valid only when eight consecutive samples with the new level have been detected (sampled at f_{MASTER} frequency).
3. Select the edge of the active transition on the TI1 channel by writing the CC1P bit to 0 in the TIM1_CCER1 register (rising edge in this case).
4. Program the input prescaler. In this example, the capture needs to be performed at each valid transition, so the prescaler is disabled (write the IC1PS bits to 00 in the TIM1_CCMR1 register).
5. Enable capture from the counter into the capture register by setting the CC1E bit in the TIM1_CCER1 register.
6. If needed, enable the related interrupt request by setting the CC1IE bit in the TIM1_IER register.

When an input capture occurs:

- The TIM1_CCR1 register gets the value of the counter on the active transition
- The input capture flag (CC1IF) is set. The overcapture flag (CC1OF) is also set if at least two consecutive captures occur while the flag remains uncleared.
- An interrupt is generated depending on the CC1IE bit

To handle the overcapture event (CC1OF flag), it is recommended to read the data before the overcapture flag. This avoids missing an overcapture which could occur after reading the flag and before reading the data.

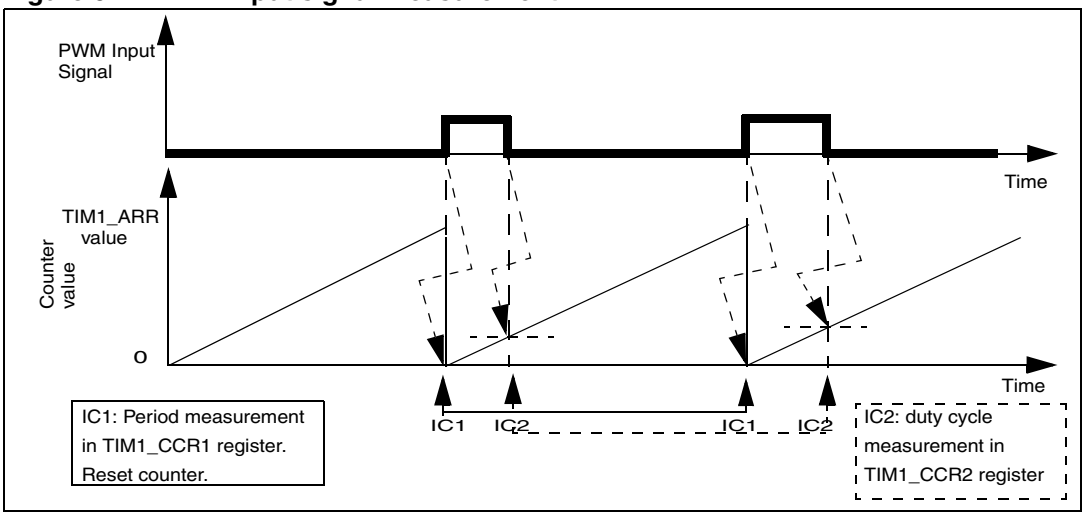
Note: IC interrupts can be generated by software by setting the corresponding CCiG bits in the TIM1_EGR register.

PWM input signal measurement

This mode is a particular case of input capture mode (see *Figure 62*). The procedure is the same except:

- Two IC*i* signals are mapped on the same TI*i* input
- These two IC*i* signals are active on edges with opposite polarity
- One of the two TI*i*FP signals is selected as trigger input and the clock/trigger controller is configured in trigger reset mode.

Figure 62. PWM input signal measurement

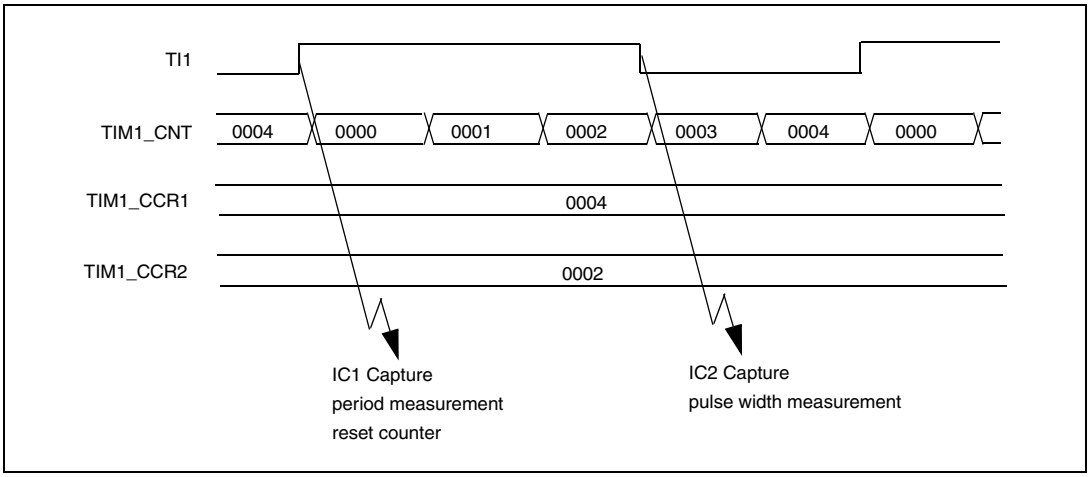


Procedure

Depending on the f_{MASTER} frequency and prescaler value, the period (in the TIM1_CCR1 register) can be measured and the duty cycle (in the TIM1_CCR2 register) of the PWM can be applied on TI1 using the following procedure:

1. Select the active input capture or trigger input for TIM1_CCR1 by writing the CC1S bits to 01 in the TIM1_CCMR1 register (TI1FP1 selected).
2. Select the active polarity for TI1FP1 (used for both capture and counter clear in TIMx_CCR1) by writing the CC1P bit to 0 (TI1FP1 active on rising edge).
3. Select the active input for TIM1_CCR2 by writing the CC2S bits to 10 in the TIM1_CCMR2 register (TI1FP2 selected).
4. Select the active polarity for TI1FP2 (used for capture in TIM1_CCR2) by writing the CC2P bit to 1 (TI1FP2 active on falling edge).
5. Select the valid trigger input by writing the TS bits to 101 in the TIM1_SMCR register (TI1FP1 selected).
6. Configure the clock/trigger controller in reset mode by writing the SMS bits to 100 in the TIM1_SMCR register.
7. Enable the captures by writing the CC1E and CC2E bits to 1 in the TIM1_CCER1 register.

Figure 63. PWM input signal measurement example



17.5.4 Output stage

The output stage generates an intermediate waveform called OC*i*REF (active high) which is then used for reference. Break functions and polarity act at the end of the chain.

Figure 64. Channel output stage block diagram