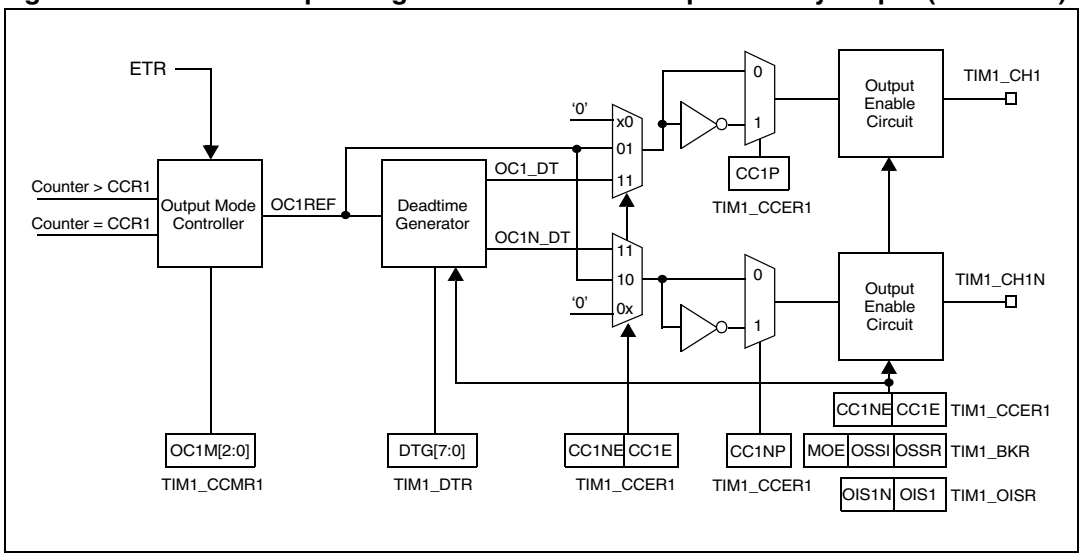
Figure 65. Detailed output stage of channel with complementary output (channel 1)



17.5.5 Forced output mode

In output mode (CC*i*S bits = 00 in the TIM1_CCMR*i* registers), each output compare signal can be forced to high or low level directly by software, independently of any comparison between the output compare register and the counter.

To force an output compare signal to its active level, write 101 in the OC*i*M bits in the corresponding TIM1_CCMR*i* registers. OC*i*REF is forced high (OC*i*REF is always active high) and the OC*i* output is forced high or low depending on the CC*i*P polarity bits.

For example, if CC*i*P = 0 (OC*i* active high) => OC*i* is forced high.

The OC*i*REF signal can be forced low by writing the OC*i*M bits to 100 in the TIMx_CCMRx registers.

Nevertheless, the comparison between the TIM1_CCR*i* shadow registers and the counter is still performed and allows the flag to be set. Interrupt requests can be sent accordingly. This is described in the output compare mode section below.

17.5.6 Output compare mode

This function is used to control an output waveform or indicate when a period of time has elapsed.

When a match is found between the capture/compare register and the counter:

- Depending on the output compare mode, the corresponding OC*i* output pin:
  - Keeps its level (OC*i*M = 000),
  - Is set active (OC*i*M = 001),
  - Is set inactive (OC*i*M = 010)
  - Toggles (OC*i*M = 011)
- A flag is set in the interrupt status register (CC*i*IF bits in the TIM1_SR1 register).
- An interrupt is generated if the corresponding interrupt mask is set (CC*i*IE bits in the TIM1_IER register).

The output compare mode is defined by the OC*i*M bits in the TIM1_CCMR*i* registers. The active or inactive level polarity is defined by the CC*i*P bits in the TIM1_CCER*i* registers.

The TIM1_CCR*i* registers can be programmed with or without preload registers using the OC*i*PE bits in the TIM1_CCMR*i* registers.

In output compare mode, the UEV has no effect on the OC*i*REF and OC*i* output. The timing resolution is one count of the counter. Output compare mode can also be used to output a single pulse.

Procedure

1. Select the counter clock (internal, external, or prescaler).
2. Write the desired data in the TIM1_ARR and TIM1_CCR*i* registers.
3. Set the CC*i*IE bits if an interrupt request is to be generated.
4. Select the output mode as follows:
   - Write OC*i*M = 011 to toggle the OC*i* output pin when CNT matches CCR*i*
   - Write OC*i*PE = 0 to disable the preload register
   - Write CC*i*P = 0 to select active high polarity
   - Write CC*i*E = 1 to enable the output
5. Enable the counter by setting the CEN bit in the TIMx_CR1 register

The TIM1_CCR*i* registers can be updated at any time by software to control the output waveform, provided that the preload registers are not enabled (OC*i*PE = 0). Otherwise, the TIMx_CCR*i* shadow registers are updated only at the next UEV (see example in *Figure 66*.

Figure 66. Output compare mode, toggle on OC1