17.5.7 PWM mode

Pulse width modulation mode allows you to generate a signal with a frequency determined by the value of the TIM1_ARR register and a duty cycle determined by the value of the TIM1_CCR*i* registers.

The PWM mode can be selected independently on each channel (one PWM per OC*i* output) by writing 110 (PWM mode 1) or 111 (PWM mode 2) in the OC*i*M bits in the TIM1_CCMR*i* registers. The corresponding preload register must be enabled by setting the OC*i*PE bits in the TIM1_CCMR*i* registers. The auto-reload preload register (in up-counting or center-aligned modes) may be optionally enabled by setting the ARPE bit in the TIM1_CR1 register.

As the preload registers are transferred to the shadow registers only when an UEV occurs, all registers have to be initialized by setting the UG bit in the TIM1_EGR register before starting the counter.

OC*i* polarity is software programmable using the CC*i*P bits in the TIM1_CCER*i* registers. It can be programmed as active high or active low. The OC*i* output is enabled by a combination of CC*i*E, MOE, OIS*i*, OSSR and OSSI bits (TIM1_CCER*i* and TIM1_BKR registers). Refer to the TIM1_CCER*i* register descriptions for more details.

In PWM mode (1 or 2), TIM1_CNT and TIM1_CCR*i* are always compared to determine whether TIM1_CCR*i* ≤ TIM1_CNT or TIM1_CNT≤ TIM1_CCR*i* (depending on the direction of the counter).

The timer is able to generate PWM in edge-aligned mode or center-aligned mode depending on the CMS bits in the TIM1_CR1 register.

PWM edge-aligned mode

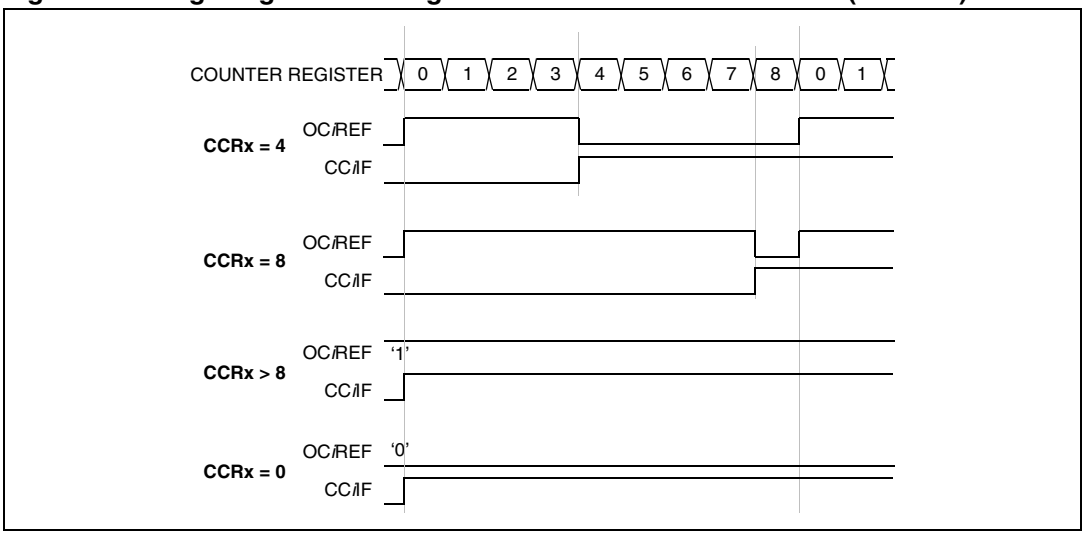
Up-counting configuration

Up-counting is active when the DIR bit in the TIM1_CR1 register is low.

Example

This example uses PWM mode 1. The reference PWM signal, OC*i*REF, is high as long as TIM1_CNT < TIM1_CCR*i*. Otherwise, it becomes low. If the compare value in TIM1_CCR*i* is greater than the auto-reload value (in TIM1_ARR) then OC*i*REF is held at 1. If the compare value is 0, OC*i*REF is held at 0. *Figure 67* shows some edge-aligned PWM waveforms in an example where TIM1_ARR = 8.

Figure 67. Edge-aligned counting mode PWM mode 1 waveforms (ARR = 8)



Down-counting configuration

Down-counting is active when the DIR bit in the TIM1_CR1 register is high. Refer to *Down-counting mode on page 139*

In PWM mode 1, the reference signal OC*i*REF is low as long as TIM1_CNT> TIM1_CCR*i*. Otherwise, it becomes high. If the compare value in the TIM1_CCR*i* registers is greater than the auto-reload value in the TIM1_ARR register, OC*i*REF is held at 1. Zero percent PWM is not possible in this mode.

PWM center-aligned mode

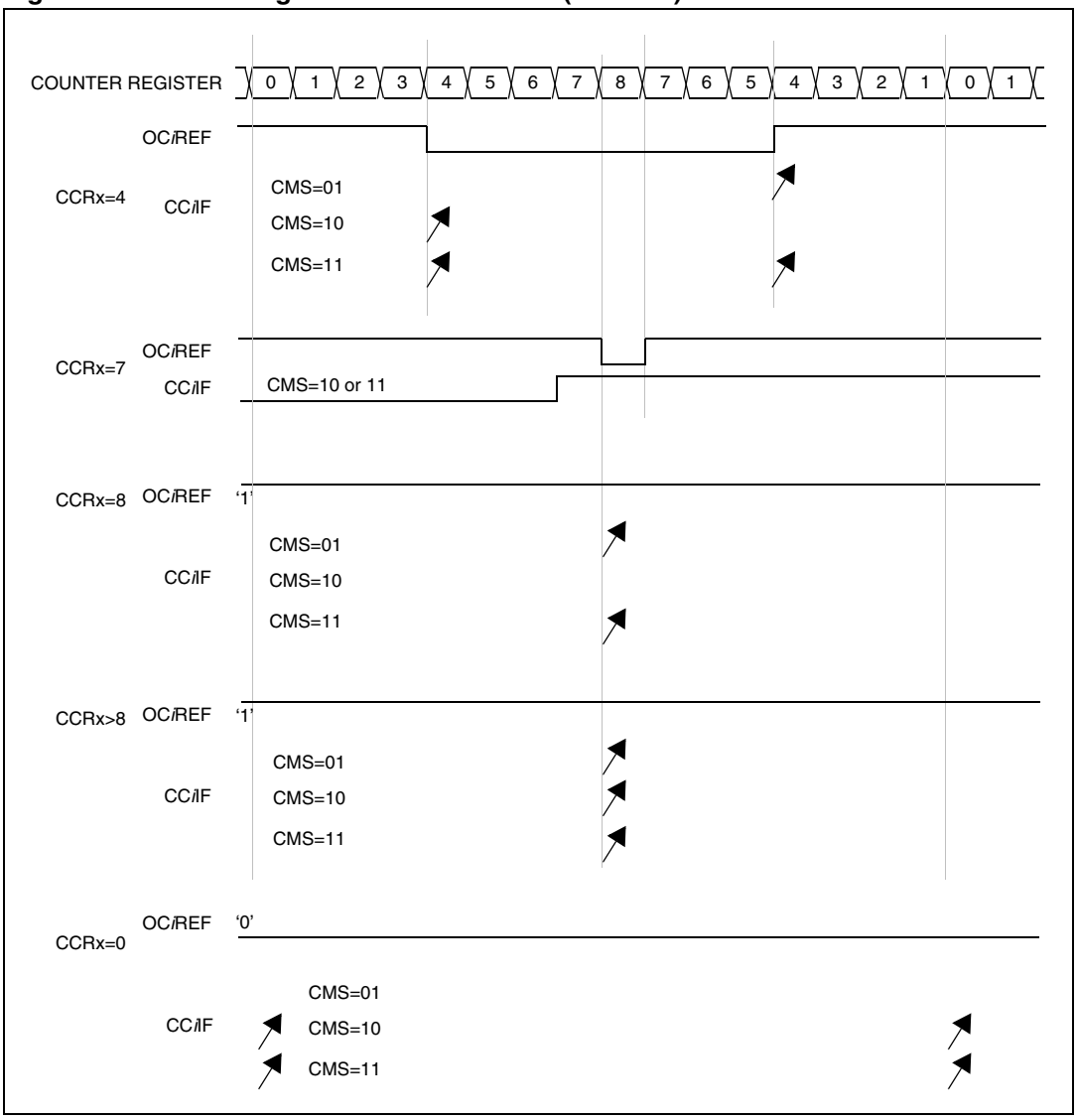
Center-aligned mode is active when the CMS bits in the TIM1_CR1 register are different from 00 (all the remaining configurations have the same effect on the OC*i*REF/OC*i* signals).

The compare flag is set when the counter counts up, down, or up and down depending on the CMS bits configuration. The direction bit (DIR) in the TIM1_CR1 register is updated by hardware and is read-only in this mode (refer to *Center-aligned mode (up/down counting) on page 141*).

Figure 68 shows some center-aligned PWM waveforms in an example where:

- TIM1_ARR = 8,
- PWM mode is PWM mode 1
- The flag is set (arrow symbol in *Figure 68*) in three different cases:
  - When the counter counts down (CMS = 01)
  - When the counter counts up (CMS = 10)
  - When the counter counts up and down (CMS = 11)

Figure 68. Center-aligned PWM waveforms (ARR = 8)



One pulse mode

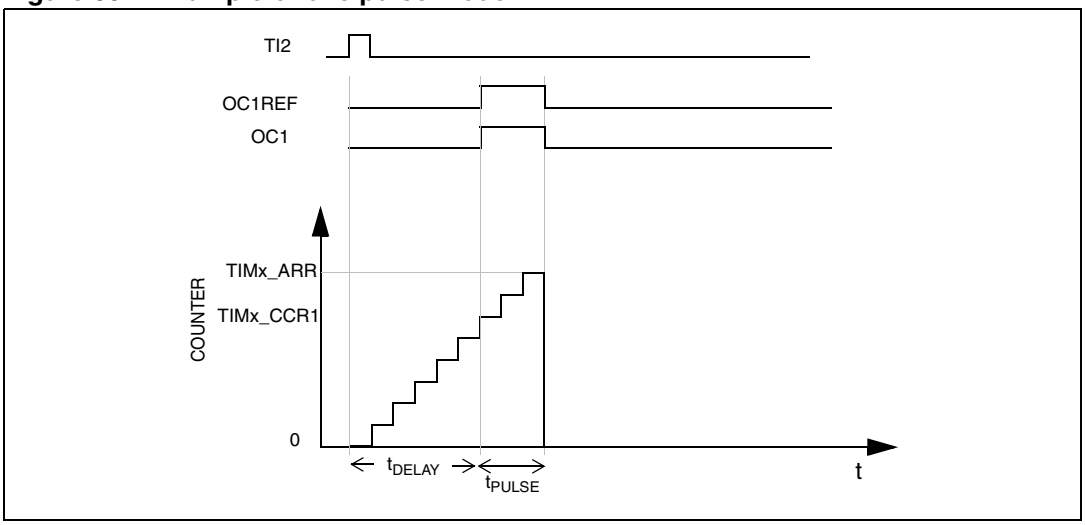
One pulse mode (OPM) is a particular case of the previous modes. It allows the counter to be started in response to a stimulus and to generate a pulse with a programmable length after a programmable delay.

Starting the counter can be controlled through the clock/trigger controller. Generating the waveform can be done in output compare mode or PWM mode. Select one pulse mode by setting the OPM bit in the TIM1_CR1 register. This makes the counter stop automatically at the next UEV.

A pulse can be correctly generated only if the compare value is different from the counter initial value. Before starting (when the timer is waiting for the trigger), the configuration must be:

- In up-counting: CNT< CCR*i* ≤ ARR (in particular, 0 < CCR*i*),
- In down-counting: CNT> CCR*i*

Figure 69. Example of one pulse mode



Example

This example shows how to generate a positive pulse on OC1 with a length of t_{PULSE} and after a delay of t_{DELAY} as soon as a positive edge is detected on the TI2 input pin.

Follow the procedure below to use IC2 as trigger 1:

- Map IC2 on TI2 by writing CC2S = 01 in the TIM1_CCMR2 register
- IC2 must detect a rising edge, so write CC2P = 0 in the TIM1_CCER1 register
- Configure IC2 as trigger for the clock/trigger controller (TRGI) by writing TS = 110 in the TIM1_SMCR register.
- IC2 is used to start the counter by writing SMS to 110 in the TIM1_SMCR register (trigger mode).

The OPM waveform is defined by writing the compare registers (taking into account the clock frequency and the counter prescaler) as follows:

- The t_{DELAY} is defined by the value written in the TIM1_CCR1 register
- The t_{PULSE} is defined by the difference between the auto-reload value and the compare value (TIM1_ARR - TIM1_CCR1).
- To build a waveform with a transition from 0 to 1 when a compare match occurs and a transition from 1 to 0 when the counter reaches the auto-reload value, enable PWM mode 2 by writing OC*i*M = 111 in the TIM1_CCMR1 register. Alternatively, enable the preload registers by writing OC1PE = 1 in the TIM1_CCMR1 register and ARPE = 0 in the TIM1_CR1 register (optional). In this case, write the compare value in the TIM1_CCR1 register and write the auto-reload value in the TIM1_ARR register. Then, generate an update by setting the UG bit and wait for an external trigger event on TI2. CC1P is written to 0 in this example.

In the example outlined above, the DIR and CMS bits in the TIM1_CR1 register should be low.

As only one pulse is required, write 1 in the OPM bit in the TIM1_CR1 register to stop the counter at the next UEV (when the counter rolls over from the auto-reload value back to 0).

Particular case: OCi fast enable

In one pulse mode, the edge detection on the TI*i* input sets the CEN bit which enables the counter. Then, a comparison between the counter and the compare value makes the output toggle. However, several clock cycles are needed for these operations and this affects the the minimum delay (t_{DELAY} min) that can be obtained.

To output a waveform with the minimum delay, set the OC*i*FE bits in the TIM1_CCMR*i* registers. OC*i*REF (and OC*i*) are forced in response to the stimulus, without taking the comparison into account. The new level of OC*i*REF (and OC*i*) is the same as if a compare match had occured. The OC*i*FE bits acts only if the channel is configured in PWM1 or PWM2 mode.

Complementary outputs and deadtime insertion

TIM1 can output two complementary signals per channel. It also manages the switching-off and switching-on instants of the outputs (see *Figure 28: TIM1 general block diagram on page 134*).

This time is generally known as deadtime. Deadtimes must be adjusted depending on the characteristics of the devices connected to the outputs (example, intrinsic delays of level-shifters, delays due to power switches).

The polarity of the outputs can be selected (main output OC*i* or complementary OC*i* N) independently for each output. This is done by writing to the CC*i* P and CC*i* NP bits in the TIM1_CCER*i* registers.

The complementary signals OC*i* and OC*i* N are activated by a combination of several control bits: The CC*i* E and CC*i* NE bits in the TIM1_CCER*i* register and, if the break feature is implemented, the MOE, OIS*i*, OIS*i* N, OSSI, and OSSR bits in the TIM1_BKR register. Refer to *Table 34: Output control for complementary OCi and OCiN channels with break feature on page 198* for more details. In particular, the deadtime is activated when switching to the IDLE state (when MOE falls to 0).

Deadtime insertion is enabled by setting the CC*i* E and CC*i* NE bits, and the MOE bit if the break circuit is present. Each channel embeds an 8-bit deadtime generator. It generates two outputs: OC*i* and OC*i* N from a reference waveform, OC*i* REF. If OC*i* and OC*i* N are active high:

- The OC*i* output signal is the same as the reference signal except for the rising edge, which is delayed relative to the reference rising edge.
- The OC*i* N output signal is the opposite of the reference signal except for the rising edge, which is delayed relative to the reference falling edge.

If the delay is greater than the width of the active output (OC*i* or OC*i* N), the corresponding pulse is not generated.

Figure 70, *Figure 71*, and *Figure 72* show the relationships between the output signals of the deadtime generator and the reference signal OC*i* REF (where CC*i* P = 0, CC*i* NP = 0, MOE = 1, CC*i* E = 1, and CC*i* NE = 1 in these examples)

Figure 70. Complementary output with deadtime insertion

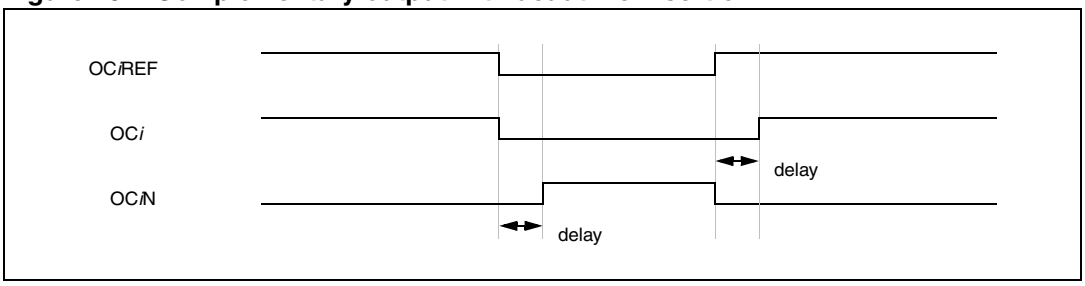


Figure 71. Deadtime waveforms with a delay greater than the negative pulse

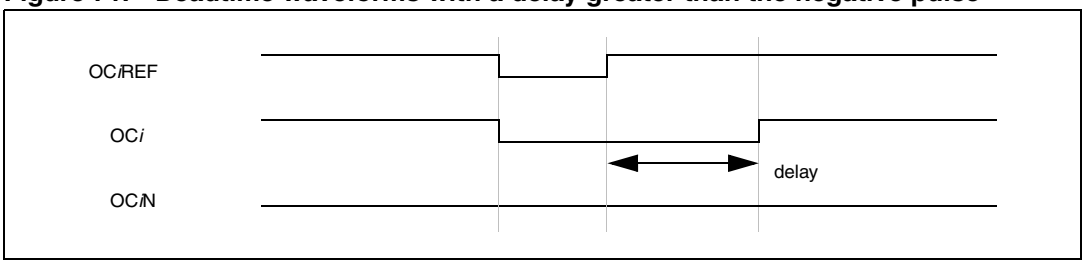
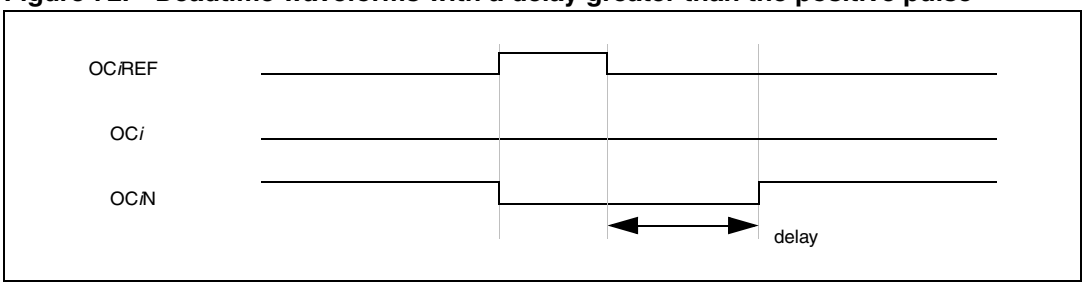


Figure 72. Deadtime waveforms with a delay greater than the positive pulse



The deadtime delay is the same for each of the channels and is programmable with the DTG bits in the TIM1_DTR register. Refer to *Section 17.7.31: Deadtime register (TIM1_DTR) on page 208* for delay calculation.

Re-directing OC*i*REF to OC*i* or OC*i*N

In output mode (forced, output compare, or PWM), OC*i*REF can be re-directed to the OC*i* or OC*i*N outputs by configuring the CC*i*E and CC*i*NE bits in the corresponding TIM1_CCER*i* registers. This means bypassing the deadtime generator which allows a specific waveform (such as PWM or static active level) to be sent on one output while the complementary output remains at its inactive level. Alternative possibilities are to have both outputs at inactive level or both outputs active and complementary with deadtime.

Note: When only OCiN is enabled (CCiE = 0, CCiNE = 1), it is not complemented and becomes active as soon as OCiREF is high. For example, if CCiNP = 0 then OCiN = OCiREF. On the other hand, when both OCi and OCiN are enabled (CCiE = CCiNE = 1), OCi becomes active when OCiREF is high whereas OCiN is complemented and becomes active when OCiREF is low.

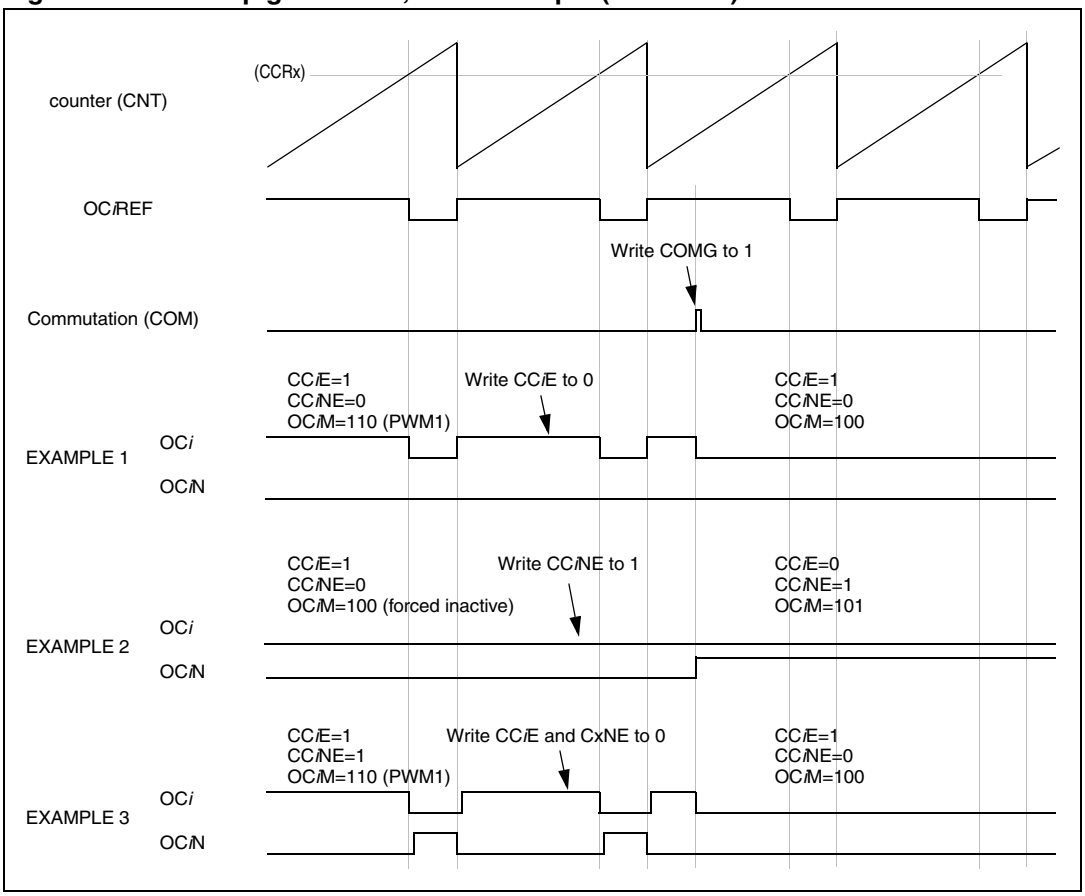
Six-step PWM generation for motor control

When complementary outputs are implemented on a channel, preload bits are available on the OC*i* M, CC*i* E and CC*i* NE bits. The preload bits are transferred to the active bits at the commutation event (COM). This allows the configuration for the next step to be programmed in advance and for configuration of all the channels to be changed at the same time. The COM event can be generated by software by setting the COMG bit in the TIM1_EGR register or by hardware trigger (on the rising edge of TRGI).

A flag is set when the COM event occurs (COMIF bit in the TIM1_SR register) which can generate an interrupt (if the COMIE bit is set in the TIM1_IER register).

Figure 73 shows the behavior of the OC*i* and OC*i* N outputs when a COM event occurs, for three different examples of programmed configurations.

Figure 73. Six-step generation, COM example (OSSR = 1)



17.5.8 Using the break function

The break function is often used in motor control. When using the break function, the output enable signals and inactive levels are modified according to additional control bits (MOE, OSSR and OSSI bits in the TIM1_BKR register).

When exiting from reset, the break circuit is disabled and the MOE bit is low. The break function is enabled by setting the BKE bit in the TIM1_BKR register. The break input polarity can be selected by configuring the BKP bit in the same register. BKE and BKP can be modified at the same time.

Because MOE falling edge can be asynchronous, a resynchronization circuit has been inserted between the actual signal (acting on the outputs) and the synchronous control bit (accessed in the TIM1_BKR register). It results in some delays between the asynchronous and the synchronous signals. For example, if MOE is written to 1 after it has been low, a delay (dummy instruction) must be inserted before it can be read correctly.

When a break occurs (selected level on the break input):

- The MOE bit is cleared asynchronously, putting the outputs in inactive state, idle state, or reset state (selected by the OSSI bit). This happens even if the MCU oscillator is off.
- Each output channel is driven with the level programmed in the OIS*i* bits in the TIM1_OISR register as soon as MOE = 0. If OSSI = 0, the timer releases the enable output otherwise the enable output remains high.
- When complementary outputs are implemented:
  - The outputs are first put in inactive state (depending on the polarity). This is done asynchronously so that it works even if no clock is provided to the timer.
  - If the timer clock is still present, the deadtime generator is reactivated to drive the outputs with the level programmed in the OIS*i* and OIS*i* N bits after a deadtime. Even in this case, OC*i* and OC*i* N cannot be driven to their active level together. Note that because of the resynchronization on MOE, the deadtime duration is a bit longer than usual (around two 2 ck_tim clock cycles).
- The break status flag (BIF bit in the TIM1_SR1 register) is set. An interrupt can be generated if the BIE bit in the TIM1_IER register is set.
- If the AOE bit in the TIM1_BKR register is set, the MOE bit is automatically set again at the next UEV. This can be used to perform a regulation. Otherwise, MOE remains low until it is written to 1 again. In this case, it can be used for security and the break input can be connected to an alarm from power drivers, thermal sensors, or any security components.

Note: The break inputs act on signal level. Thus, the MOE bit cannot be set while the break input is active (neither automatically nor by software). In the meantime, the status flag BIF cannot be cleared.

The break can be generated by the break input (BKIN) which has a programmable polarity and can be enabled or disabled by setting or resetting the BKE bit in the TIM1_BKR register.

In addition to the break inputs and the output management, a write protection has been implemented inside the break circuit to safeguard the application. It allows the configuration of several parameters (OC*i* polarities and state when disabled, OC*i*M configurations, break enable, and polarity) to be frozen. Three levels of protection can be selected using the LOCK bits in the TIM1_BKR register. The LOCK bits can be written only once after an MCU reset.

Figure 74 shows an example of the behavior of the outputs in response to a break.

Figure 74. Behavior of outputs in response to a break (channel without complementary output)