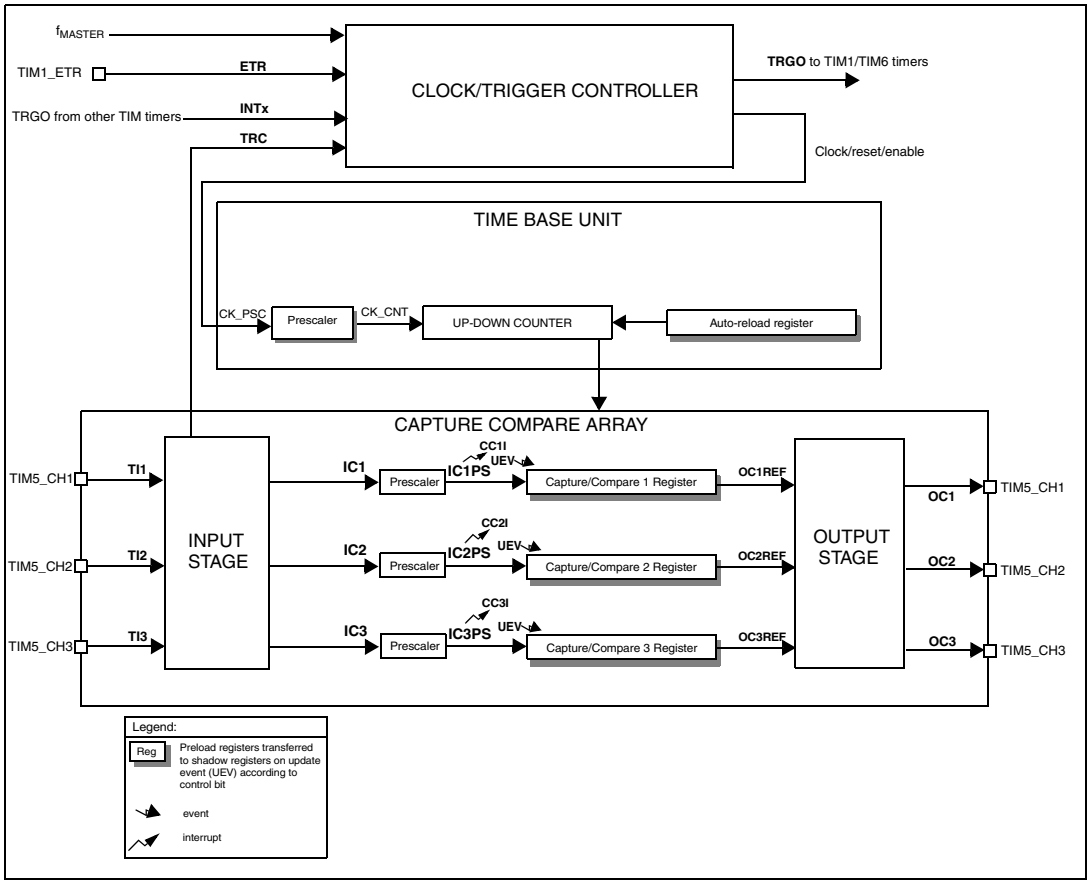
Figure 80. TIM5 block diagram



18.4.1 Time base unit

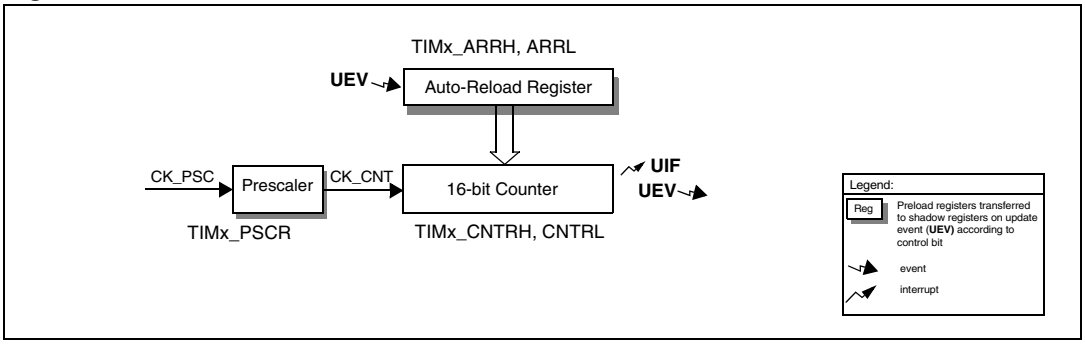
The timer has a time base unit that includes:

- 16-bit up counter
- 16-bit auto-reload register
- 4-bit programmable prescaler

There is no repetition counter.

The clock source for is the internal clock (f_{MASTER}). It is connected directly to the CK_PSC clock that feeds the prescaler driving the counter clock CK_CNT.

Figure 81. Time base unit



For more details refer to *Section 17.3: TIM1 time base unit on page 135*.

Prescaler

The prescaler implementation is as follows:

- The prescaler is based on a 16-bit counter controlled through a 4-bit register (in the TIMx_PSCR register). It can be changed on the fly as this control register is buffered. It can divide the counter clock frequency by any power of 2 from 1 to 32768.

  The counter clock frequency is calculated as follows:

  $f_{CK\_CNT} = f_{CK\_PSC}/2^{(PSCR[3:0])}$

The prescaler value is loaded through a preload register. The shadow register, which contains the current value to be used is loaded as soon as the LS Byte has been written.

The new prescaler value is taken into account in the following period (after the next counter update event).

Read operations to the TIMx_PSCR registers access the preload registers, so no special care needs to be taken to read them.

Counter operation

Refer to *Section 17.3.4: Up-counting mode on page 137*.

18.4.2 Clock/trigger controller

A clock/trigger controller and the associated TIMx_CR2 and TIMx_SMCR registers are not implemented in TIM2/TIM3, only in TIM5. Refer to *Section 17.4: TIM1 clock/trigger controller on page 145*